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# 1 Document Conventions

1.1 In this Service Manual certain conventions are used to indicate where precautions are required.

1.2 The following provides an example of a warning.

***Warning – Do not dispose of cells in fire.***

Failure to observe a warning may result in injury or death.

1.3 The following provides an example of a caution.

***Caution – Do not short-circuit the terminals of the battery pack.***

Failure to observe a caution may result in damage to equipment.

1.4 The following provides an example of a notice.

***Note - Check the integrity of the coaxial cable before making SINAD measurements***

Notes are provided as advice and guidance to service personnel.

# 2 Service Levels

2.1 Tellit Communications Limited provides support to Service Engineers who have been approved and trained for the maintenance of its products. Three levels of service are provided as follows:


2.2 Service Level 1 – This service level applies if the Distributor's personnel have received no product specific training or if the perceived fault is outside the Distributor's level of competence. An equivalent product from the Company's exchange stock held by the Distributor will replace the product.


2.3 Service Level 2 – This service level applies if the Distributor's personnel been trained and authorised to perform service to level 2 on the product. This level enables the Distributor to replace parts down to module level. Typically this would include replacing external mechanical parts, replacing speaker, microphone, LCD Display panel etc.


2.4 Service Level 3 – This service level applies if the Distributor's personnel have been trained and authorised to perform service to level 3 on the product. This level provides for service down to electrical component level. Products having faulty PCBs or other components may be repaired as required.

# 3 Product Description

3.1 The A66 is a compact high performance Low Emission Mobile Station (LEMS) intended for use within mobile networks conforming to the Nordic Mobile Telephone 450 MHz (NMT 450) standard. Several versions of the A66, as detailed in Table 3-1, are provided intended for use in a variety of national versions of the NMT 450 system. These different versions of the equipment use different transmit and receive radio frequencies as required for use in the country specific versions of the NMT 450 system.

3.2 To be continued!

# 4 Technical Specification

4.1 Environmental

Operational Temperature Range: -10°C to +55°C
Transmitter:
RF Power Output: 100 mW ± 3dB
Maximum Frequency Error: ± 2.5 kHz, -10°C to +55°C
Spurious Emissions:

| | 100 kHz – 1GHz | 1-4 GHz |
|---|---|---|
| Transmitter ON | <0.25 uW | <1 uW |
| Transmitter in standby mode | <2 nW | <20 nW |

Maximum frequency deviation: ± 4.7 kHz
Adjacent channel power: Better than 70 dB below carrier
Tx Harmonic distortion: <5%

4.2 Supervisory Tone Deviation ±300 Hz Nominal.

4.3 Receiver:

RF Sensitivity – 117 dBm (20 dB SINAD) +15°C to +45°C
- 114 dBm (20 dB SINAD) –10°C to +15°C and +35°C to +55°C
Duplex Sensitivity Degradation: <3 dB
Adjacent channel selectivity: >64 dB under normal test conditions (+15° to +35°C)
>60 dB under extreme conditions (-10°C and +55°C)
Spurious response rejection: >67 dB outside NMT band; >60 within
Intermodulation Rejection: >63 dB
Blocking Level: >85 dBuV EMF

4.4 Spurious emissions:

| 100 kHz – 1GHz | 1 GHz – 4 GHz |
|---|---|
| < 2 nW | < 20 nW |

Harmonic distortion: < 5%

| Country | Band | TX Start Channel | TX Stop Channel | Channel Numbering | Start Freq TX Extended Band | Stop Freq TX Extended Band | Channel Numbering Extended Band | Reverse Channel Numbering | Channel Spacing | Interleaving | Y1 | Y3 | Z | International Prefix | Country Code |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Romania | 1:3 | 453.000 | 457.475 | 1 - 180 | | | | | 25 kHz | No | 5 | 3 | 4 | | |

Table 3-1

# 5 Recommended Tools and Materials

**All service to be carried out on an**
**Anti-Static Workbench complete with the following:**
**Conductive work surface and Wrist strap**

2

5.1 **Level 2 Service** - The following hand tools will be required:

5.1.1 Small Torx™ screwdriver size T6 X 60

5.1.2 Torque Driver with T6 X 60 adapter – with torque range set to 0.32 Nm

5.1.3 Small Jeweller's screwdriver

5.1.4 Small tweezers

5.2 The following consumable materials will be required:

5.2.1 Anti-Stat foam cleaner – Ambersil or Servisol

5.2.2 IPA – RS 106-970

5.2.3 Anti-Static bags

3

5.3 **Level 3 Service** – The following additional hand tools will be required:

5.3.1 Small side cutters

5.3.2 Small fine pointed tweezers – RS 549-628

5.3.3 Soldering/desoldering station – SMD soldering and rework – Metcal SP200 SMT – 1160 Hako

5.3.4 Scalpel Swan Morton No 5 + Blades

5.3.5 Bench Light Magnifier

5.4 The following consumable materials will be required:

5.4.1 Solder wire – LMP Sn63 Pb 37 ∅ 0.4mm. Or Multicore Smart wire RS 419-503

5.4.2 Solder Wick – Chemwick

5.4.3 Flux pen Alpha Metals NR205

5.4.4 Stiff cleaning brush

5.4.5 Soldering Iron tip cleaner – RS561-533

# 6 Recommended Test Equipment

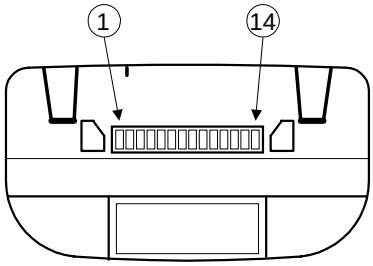
6.1 The following test equipment will be required:

| Item | Description | Tellit P/n | Qty | Remarks |
|---|---|---|---|---|
| 1 | IBM Compatible PC with Pentium 100 or higher fitted with 32 MB RAM and CD ROM Drive and Mouse. | | 1 | |
| 2* | Cable Assembly 9W D Plug – 9W D Socket. | xxxxx | 1 | |
| 3* | Cable Assembly 25W D Plug – 25W D Socket. | xxxxx | 1 | |
| 4* | Mains Charger | xxxxx | 1 | |
| 5 | RF Communications Test Set | | 1 | HP 8920B or similar |
| 6* | Cable Assembly 50Ω SMA Plug - 50Ω A66 Antenna Connector | xxxxx | 1 | |
| 7 | Power Supply Unit 12V dc Hum & Noise <50 mV pp | | 1 | |
| 8* | Test Interface Box A66/A77 | xxxxx | 1 | |
| 9* | Cable Assembly 37W D Plug – 37W D socket | xxxxx | 1 | |
| 10* | Test Fixture A66 Phone | xxxxx | 1 | |
| 11* | Test Fixture A66 PCB | xxxxx | 1 | |
| 12 | Coaxial Adapter SMA Socket – N Plug | | 1 | |
| 13* | Coaxial Lead Assembly 50Ω BNC Plug - 50Ω BNC Plug | xxxxx | 1 | |
| 14 | Digital Multimeter | | 2 | |
| 15* | Test Lead 4mm Plug – 4mm Plug Red | xxxxx | 3 | |
| 16* | Test Lead 4mm Plug – 4mm Plug Black | xxxxx | 3 | |

6.2 Items marked with an asterisk are available from Tellit either individually, quoting the Tellit p/n given in the table above or as a complete kit quoting Tellit p/n xxxxx.

# 7 Circuit Operational Descriptions

## I/O Specification for A66 terminal




| PIN # | NAME | FUNCTION IN A66 | LEVELS |
|---|---|---|---|
| 1 | CHG_IN | Positive charge voltage (INPUT) | +5.7V to + 6.2Volt Current limited to 800mA +/-10% |
| 2 | CHG_IN | Used in parallel with pin 1 | |
| 3 | ID | External resistor value to GND. Indicates accessory connected. | Portable Handsfree = 10kohm +/-1% Service equipment=120k +/-1% (22,33,56,82k are future values) |
| 4 | TXD | Asynchronous data / MISO (OUTPUT) | HIGH= Min 2.2V @ 2mA LOW= Max 0.7V @ 2mA |
| 5 | SCK | **SPI buss clock (INPUT) | 1.6V < HIGH < 3.3V -0.5V ≤ LOW ≤ 0.5V |
| 6 | RXD | Asynchronous data / MOSI (INPUT) | 1.6V < HIGH < 3.3V -0.5V ≤ LOW ≤ 0.5V |
| 7 | * HOOK_C<br>or<br>RESET | Hook control Not for placing outgoing calls! Pull-up, 100k to +3V<br>Negative voltage puts phone into Reset mode. (INPUT) | 1.6V < HIGH < 3.3V -0.5V ≤ LOW ≤ 0.5V Low > 60ms changes state<br>-2V to -4V |
| 8 | HOOK | Hook status indication (OUTPUT) | HIGH= Min 2.2V @ 2mA LOW = Max 0.7V @ 2mA Off hook = HIGH |
| 9 | +3VDIG | +3V (OUTPUT) | ≥ 2.7 Volt @ Max 2mA |
| 10 | AF_OUT | Analog audio (OUTPUT) | 1Khz@ +/-3kHz dev = 45mVRMS (EMF) Can drive >10k//<50pF |
| 11 | AGND | Analog ground | 0 volt |
| 12 | AF_IN | Analog audio AC coupled (INPUT) | 1kHz @ 250mVRMS = ± 3kHz dev $Z_{in}$> 100k |
| 13 | GND | Used in parallel with pin 14 | |
| 14 | GND | Charger ground | 0 volt |

Table 7-1

* Only this function in headset mode.
** Used for serial for programming only. // = In parallel with

## Circuit Operational Description - Connections

7.1 System Connector

The connections to the System Connector J104 are defined in Table 7-1 above.

7.2 Level Translator/Decoder

Level Translator comprising transistors Q101, Q102 and Q103 provide level translation and decoding between the **HOOK_C/REST** signal derived from externally connected equipment, and the **HOOK_C** and **RESET** internal lines. The level on **HOOK_C/RESET** is decoded according the following truth table:

| HOOK_C/RESET | HOOK_C | RESET |
|---|---|---|
| +3V | 0 | 1 |
| 0V | 1 | 1 |
| -4.5V | 1 | 0 |

The **HOOK_C/RESET** line is pulled high resistors R116 and R117 to +3 V. Under both normal and test modes of operation the **HOOK_C/RESET** line is ether allowed to be pulled up, by the pull up resistor, or pulled low to 0V by an external device. When the line is pulled to –4.5 V, by an external device, the **/RESET** line goes to logic level 0.

The /RESET line is input to the reset input to the microprocessor U301 pin 20. Thus a level of –4.5 V on HOOK_C/REST causes the microprocessor to execute a reset cycle.

7.3 LCD Module

The LCD Module is connected via J102. Data lines **SCL** – Serial Clock, and **SDA** – Serial Data, provide a serial data interface from the microprocessor U301 to the LCD Module. The. microprocessor writes to the display over these lines.

7.4 Battery Pack Interface

Interface to the Battery Pack is via connector J101. The connections to J101 are defined in figure 7-1.

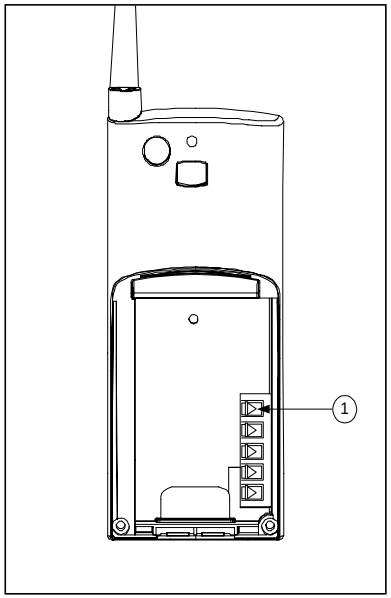
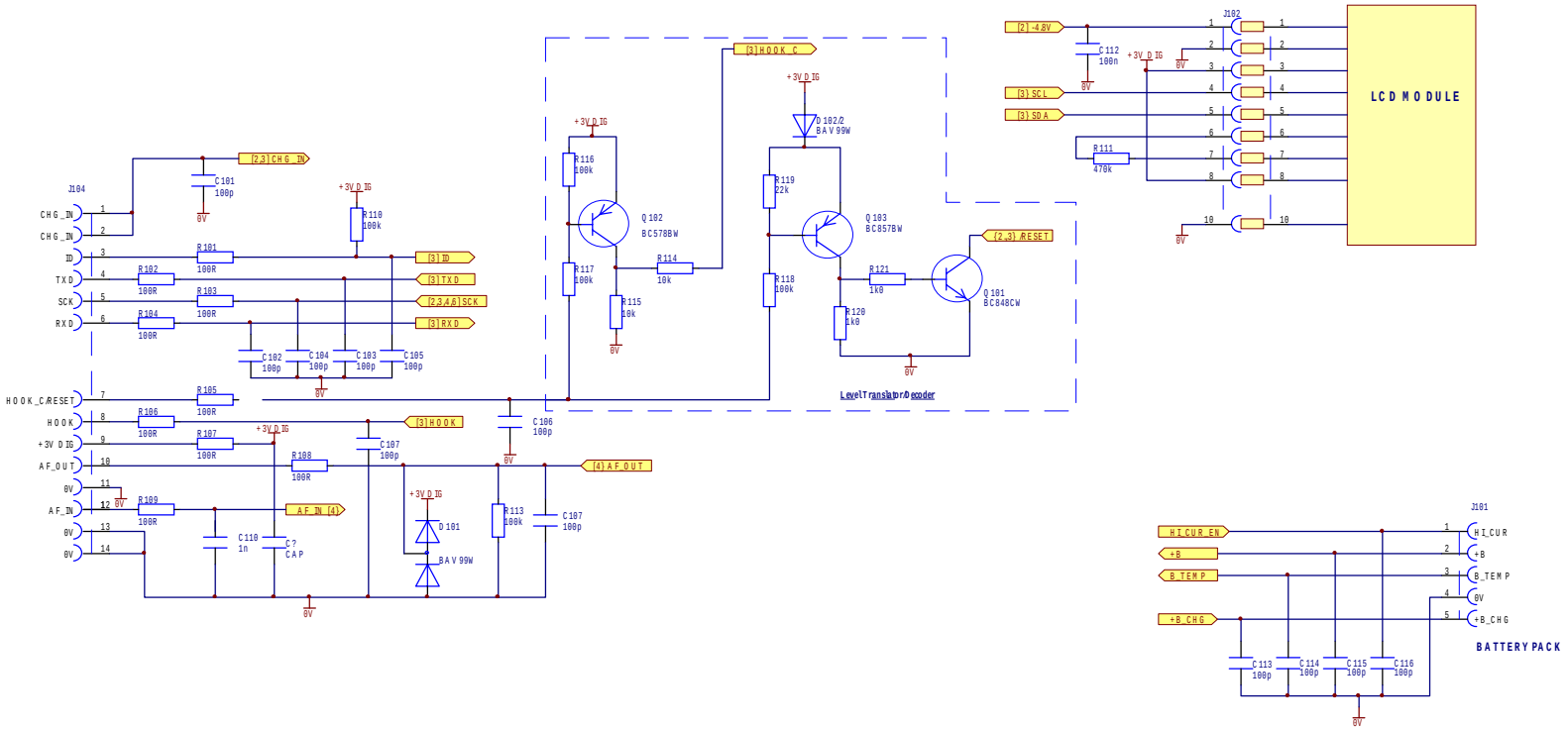



Figure 7-1




**Circuit Diagram - A66**
**Connections**

## Circuit Operational Description - Power

### 7.5 Power On

The supply input to U201 is derived from the output of the Battery Pack via line **+B**. A voltage of at least 1.5 V is present on this line whenever a battery pack is connected to the phone or if the phone is connected to a charger. With the phone switched off the line **/+BATT_ON** is pulled high via a pull up resistor within U210 connected to pin 48. Under the initial condition the **/RESET** line is held low.
The normal power on sequence is initiated when the user presses the **ON** key shown on the Processors circuit. Pressing the ON key causes transistor Q301 on the Processor circuit to turn on pulling the **/+BATT_ON** line low. Simultaneously signal line **B_TEMP** on the Processor circuit pulled high via diode D314. The signal B_TEMP is routed to the Battery Pack via J101 pin 3 on the Connections circuit and causes the DC/DC Converter stage within the Battery Pack to start-up thus outputting a voltage of +3.3 V to the **+B** line. The +B line provides power supply to U201.
When U201 recognises that **/+BATT_ON** is low it checks the output voltage of LDO Reg L. If the output voltage of regulator LDO Reg L is above 2.93 V i.e. the regulator is producing an output voltage above the Under Voltage Lockout (UVLO) a time out period of 250 ms is started. At the end of this 250 ms period the /RESET line goes high which releases the reset condition from the microprocessor thus allowing normal program execution to proceed.

### 7.6 Power Off

U202 comprises an 8-bit serial input shift register with output storage. Data is shifted into the register under control of the microprocessor U201 using lines **LE_595**, **DATA_OUT** and **SCK**. As part of its power on routine the microprocessor writes logic 1 to the Q5 bit of the shift register. Thus Q5 output of Q202 is at logic level high. The **/OFF** signal (U201 pin 33) is derived from the Q5 output of U202.
When a power down sequence is initiated the microprocessor U201 clears bit Q5 of the shift register. The logic level at U201 pin 33 thus goes to 0. U201 goes into shut down and disables its regulators at the phone powers down.

### 7.7 Regulators

Regulator LDO Reg L located within U201 provides a supply of +3V used to power the digital circuits of the phone. The regulator output voltage is present when the voltage on line **+B** is above +3.1 V.
Regulator LDO Reg A located within U201 provides a supply 0f +3V used to power the analogue circuits of the phone. The regulator is enabled under control of the microprocessor U301 via the control line **/EN_+3VA**.
–4.8 V DC/DC Converter
–4.8 V DC/DC Converter comprising U203 operates from the +3VDIG supply line and generates a supply of – 4.8 V which is fed to the LCB Module (part of Connections Circuit) via line **–4.8V**. The LCD Module requires –VE supply that is a function of the ambient temperature in order to ensure adequate display contrast over the required range of ambient temperatures. The converter circuit includes a thermistor R239 that causes the converter output voltage to vary as a function of the ambient temperature as required by the LCD Module.
The –4.8 V DC/DC Converter is enabled by the microprocessor U301 via signal line via **–4.8V_EN.**

## 7.8 Buzzer Amplifier

The Buzzer Amplifier, part of U201, comprises an audio frequency amplifier having a single ended input and bridge connected output. Buzzer tones, derived from the microprocessor U301 via the BaseBand Processor are input to the stage on signal line RINGER_IN. The output of the Buzzer Amplifier drives the Buzzer BU1.

## 7.9 Speaker Amplifier

The Speaker Amplifier, part of U201, comprises an audio frequency amplifier having a single ended input and bridge connected output. Received audio signals, derived from the BaseBand Circuit are input to the stage via signal line **SPEAKER_IN**. The output of the Speaker Amplifier drives the Speaker.

## 7.10 8-Bit Serial Register

8-bit Serial Register comprising U202 converts serial data from the microprocessor, sent via data/control lines **LE_595**, **DATA_OUT** and **SCK**, to parallel forma and latches the data at outputs Q0 –Q7. The functions of each bit is as follows:

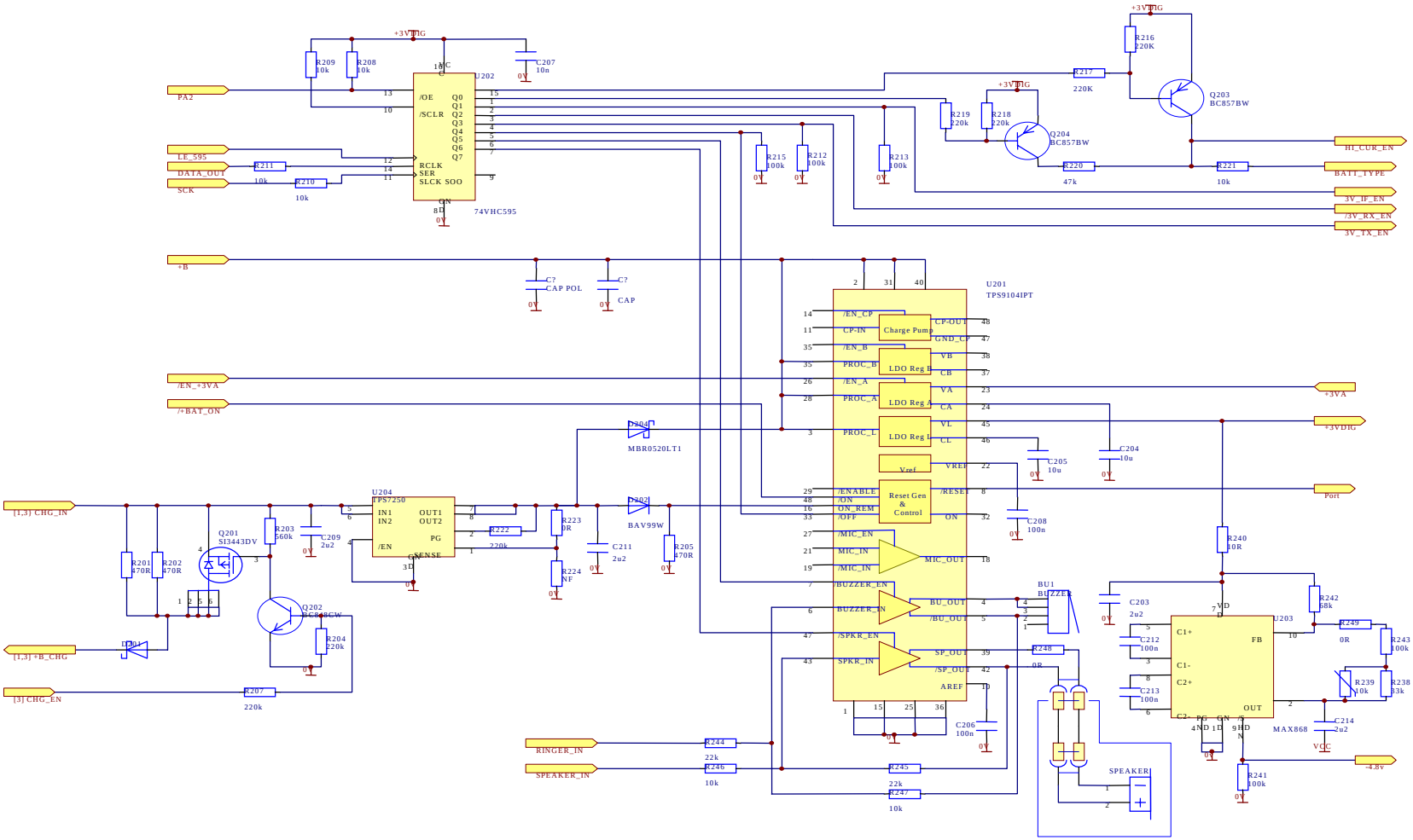
| | **Signal Name** | Description |
|---|---|---|
| Q0 | HI_CUR_EN | Enable the Battery Pack in high current mode. |
| Q1 | BATT_TYPE | Enables battery type to be read. |
| Q2 | 3V_IF_EN | Enables 3V supply to IF. |
| Q3 | /3V_RX_EN | Enables 3V supply to RX |
| Q4 | 3V_TX_EN | Enables 3V supply to TX |
| Q5 | /OFF | Power down |
| Q6 | /BUZZER_EN | Enable the buzzer |
| Q7 | /SPKR_EN | Enable the speaker |

## 7.11 +5V Regulator

The 5V Regulator comprising U204 is required in order to facilitate the operation of the phone from a charger when either no battery pack is fitted or alternatively the alkaline battery pack is fitted by its cells are discharged. Under these conditions U204 provides a regulated of 5 V that is used to power the phone.

## 7.12 Charger Control

Charger Control circuit comprises transistors Q201 and Q202. Signal line CHG_EN, derived from the microprocessor U301, turns Q201 on when fast charging is required. When fast charge is not signalled by the microprocessor by-pass resistors, R201 and R202, allow a current of the order of 25 mA to trickle into the battery pack.




**Circuit Diagram - Power**

## Circuit Operational Description - Processor

### 7.13 Microprocessor

Microprocessor U301, with the exception of the calculation of SIS, provides all data processing required within the phone. Program storage is in internal Flash Memory facilitating field program upgrades.
The Keyboard is serviced by the microprocessor under interrupts. Inputs INT0 – INT3 being the interrupt inputs. When an interrupt is serviced the processor scans the PD0-PD3 lines in order to ascertain which key has been pressed.
Output pins PA0 and PA1 drive a dual colour LED D303 providing status indicator with the following indications:
Green Continuous– Call in progress
Green Fast Flash – Incoming call
Green Slow Flash 3 Seconds – In service
Red/Green Flash - Roaming alarm
Red Flash – No service
Red Continuous – Battery low
Output pin PC7 drives transistor Q307, and Q308. Q307 controls the LEDs used to illuminate the Keyboard. Q308 drives the LEDs used to illuminate the LCD Display.
PA0 and PA1 provide a 2-wire bi-directional interface to the External EEPROM U302. Via this interface data is written to and read from the External EEPROM.
The 2-wire serial interface is also used to write data to the LCD Module, part of Connections Circuit, via signal lines **SDA** and **SCL**.
Output PA5 provides a signal to the Charger Control (part of Power Circuit) via signal line **CHG_EN** used to enable fast charging of the battery pack. A logic level high on the line enables fast charging of the battery pack.
Output PA6 provides a signal used to enable the –4.8 V DC/DC Converter (part of Power Circuit). A logic level high on the line enables the –4.8 V DC/DC Converter.
Input PA7, via Q304, is used to detect that a charger is connected to the phone. When a charger is present signal line CHG_IN, from System Connector J104 pins 1&2 will be at the charger output voltage. This voltage, via resistor R309, will cause transistor Q304 to turn on pulling input pin PA7 low. When no charger is present PA7 will be high.
Input PF0 is used to input the state of the **HOOK_C** signal derived from System Connector J104 pin 7 via Q102 on the Power Circuit. A logic level low signals off hook.
Input PF1 via signal line BATT_TYPE operates as an analogue input to the microprocessor. When the processor executes the Get_Battery_Type routine transistor Q204 on the Power Circuit is briefly turned on connecting the top end of resistor R220 to +3V. Resistor R220 in conjunction with the Battery Identity Resistor, mounted in the battery pack, form a potential divider. Analogue input PF1 reads the voltage output of the potential divider and determines battery type according to the following table:

| **Battery Type** | **ID Resistor** | **Voltage** |
|---|---|---|
| NiMH | 15k | 0.725 V |
| Alkaline | 100k | 2.04 V |

Analogue input PF2 inputs the Received Signal Strength Indicator (RSSI) signal derived from the Receiver Circuit.
Analogue input PF3 is used to input the phone's internal temperature. Temperature measuring circuit, comprising thermistor R380 and resistor R348, form a potential divider fed from the +3VDIG supply. Thus the nominal voltage input to PF3 is a function of internal temperature according to the following table:

| Temperature | Voltage |
|---|---|
| -10°C | 2.452 V |
| 0°C | 2.215 V |
| +10°C | 1.940 V |
| +20°C | 1.646 V |
| +30°C | 1.358 V |
| +40°C | 1.094 V |
| +50°C | 0.867 V |
| +60°C | 0.680 V |

Input PF4 – Not implemented.
Analogue input PF5 is used to monitor the temperature of the Battery Pack. Such measurement is required as part of the battery management's charge termination algorithm and also to ensure that fast charging is disallowed if the cell temperature is less that 0°C or greater than +45°C. The following table shows the typical relationship between cell temperature and the nominal voltage at PF5.

| Cell Temp | Voltage at PF5 |
|---|---|
| -10°C | 2.563 V |
| 0°C | 2.342 V |
| +10°C | 2.086 V |
| +20°C | 1.822 V |
| +30°C | 1.577 V |
| +40°C | 1.366 V |
| +50°C | 1.202 V |

Analogue input PF6 is used to measure the battery pack cell voltage. When the +3VDIG supply is present, i.e. phone powered on, transistor Q306 is turned on thus turning on transistor Q305. With Q305 on the voltage present on signal line **+B_CHG**, which is the voltage directly across the cells, is divided by potential divider comprising resistors R313 and R317.
RXD data input to the microprocessor accepts serial data from the System Connector pin 2.
TXD data output from the microprocessor sends serial data to the System Connector pin 4.
PF7 analogue input reads the resistance between System Connector J104 pin 3 and 0V. Each type of accessory is provided with a distinctive value of ID resistor as shown in the table below. By this means the microprocessor determine which accessory is connected.

| Accessory Type | ID Resistance |
|---|---|
| Charger | Open. |
| Portable Handsfree | 10k |

PE2 outputs signal /EN+3VA that is used to enable LDO Reg A on the Power Circuit.
PE3 inputs FFSK_DET from the FFSK Demodulator on the BaseBand Circuit. FFSK_DET indicates that FFSK data is being received.
PE4 inputs TX_DATA_CLK from the FFSK Modulator part of the BaseBand Circuit. Data is valid on the rising edge of TX_DATA_CLK.
PE5 inputs RX_DATA_CLK from the FFSK Demodulator part of the BaseBand Circuit. Data is valid in the rising edge of RX_DATA_CLK.
PE6 – Not used.
PE7 outputs hook status to the System Connector pin 8. Logic level high indicates off-hook.
PB0 output /CS_AKM enables the BaseBand Processor chip U410 for control over the serial lines comprising DATA_OUT, DATA_IN and SCK. A logic level low on the line enables serial communication.
**PB1** outputs serial clock **SCK** to the BaseBand Processor chip U401 and the serial clock input of the SIM Processor. Data on **DATA_IN** and **DATA_OUT**, to /from the BaseBand Processor **is** valid on the rising edge of **SCK.** The connection to the serial clock input of the SIM Processor is used to clock data into and out of that device.
PB2 outputs serial control data to the BaseBand Processor chip U401 and serial data into the SIM Processor.
PB3 inputs serial data from the BaseBand Processor chip U401and serial data from the SIM Processor.
PB4 outputs an enable signal to the SIM Processor. When enabled the SIM

Processor can communicate with the microprocessor.
PB5 outputs SYNTH_LOAD to the Synthesiser. When SYNTH_LOAD goes high data sent to the synthesiser's registers is latched into registers.
PB6 outputs LE_595 provides a latch enable signal to 8-bit Shift Register U202 on the Power Circuit. On the rising edge of LE_585 data in the shift register is transferred to the devices output latches.
PB7 outputs the buzzer signal via signal line BUZZER.
PD4 outputs TX_DATA to the FFSK Modulator part of the BaseBand Processor.
PD5 outputs TX_DATA_EN to enable the FFSK Modulator part of the BaseBand Processor for the transmission of FFSK data.
PD6 inputs **RX_DATA** from the FFSK Demodulator part of the BaseBand Processor.
PD7 – Not used.

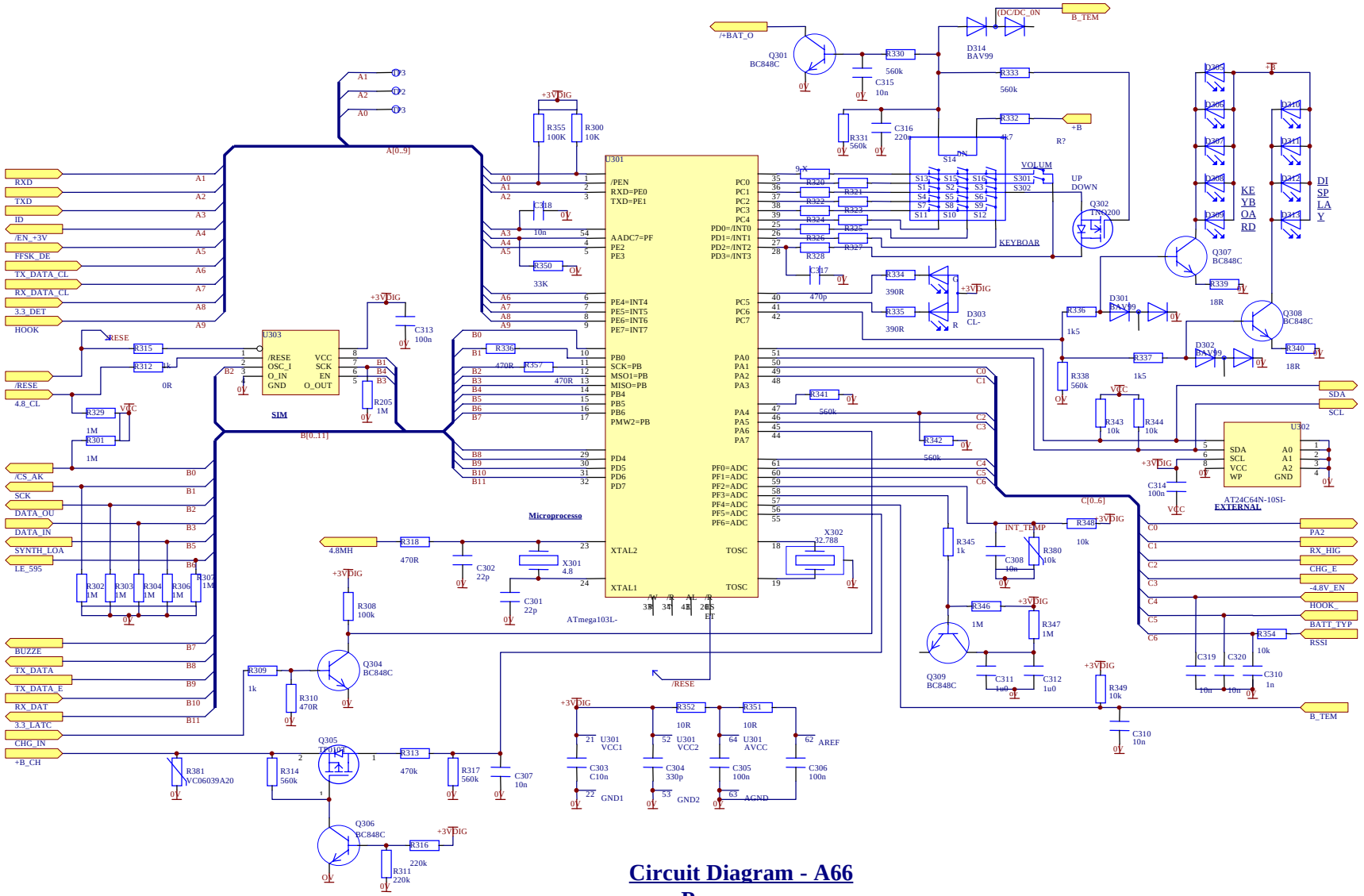
Quartz crystal X301, operating at a frequency of 4.8 MHz, provides the main clock for the microprocessor. Signal line **4.8MHz** provides clock signal to the BaseBand Processor. Ceramic resonator X302 operating at a frequency of 32.788 kHz provides a clock for the microprocessor used when in sleep mode i.e. when the phone is in power down. Operating at the lower clock rate significantly reduces the power consumption when in sleep mode.

## 7.14 SIM Processor

The SIM Processor U303 comprises an 8-bit microprocessor. Tellit programs the device with a secret authentication code (SAK). During authentication the MS receives a number RAND (Random Challenge) from the MTX. From RAND the SIM Processor calculates 2 numbers, SRES and B-Key. SRES (Signed Response) is sent to the MTX to confirm the mobile station's identity and B-key is used to encrypt the B-subscriber's number. When the SAK is programmed into the device a separate and unrelated SIM module serial number, the SIS number, is also generated. This SIS number appears on the equipment label affixed to the rear of the phone. **In the event of failure of the SIM Processor a replacement device, programmed by Tellit, must be obtained**. The replacement SIM Processor will be shipped with a replacement equipment label bearing a new SIS number. **When the phone is commissioned it is important that the old SIS number be de-registered and the new SIS number registered with the system operator.**

## 7.15 External EEPROM

The External EEPROM provides non-volatile memory for such as the Phone Book and other customer configurations.




## Circuit Diagram - A66
## Processor

## 7.16 Receive Audio

Receive audio, derived from the Demodulator is input via signal line **RX_AUDIO** into AMP2 (part of U401). Resistors R407 and R408 set the mid-band gain of the stage. The output of the stage is input the anti-aliasing filter AAF2.

The anti-aliasing filter AAF2 removes components of the receive audio at frequencies higher than twice the high frequency cut-off point of the band pass filters (above 7.8 kHz). The output of AAF2 is input to Digital Gain Control VR5.

VR5 provides a variable gain stage, controlled by the microprocessor (U301) over the serial control bus comprising **DATA_OUT, SCK**, **DATA_IN** and **/CS_AKM**. The gain of the stage may be adjusted in steps of 0.4 dB over the range –6.0 dB to +6.4 dB. The output of **VR5** is input to de-emphasis circuit **D/E**.

The de-emphasis circuit D/E provides a –6-dB/octave-frequency response over the frequency range of 300 Hz to 3.4 kHz. The output of D/E is input to switch **RXAUDION**.

Switch **RXAUDION** is controlled by the microprocessor (U301) via the serial control bus, Thus the Thus the microprocessor may mute the received audio when not required. The output of the RXAUDION is output to U401 pin 18 and thence to C414.

C424 couples the receive audio into U401 pin 9 (EXPIN). This pin provides input to the expander stage **EXP**. The expander provides amplitude expansion of the receive audio signal such for a 1 dB change in level at the expander input there is a 2 dB change in level at the expander output. The expander may be by-passed by means of switch **EXPON** under control of the microprocessor (U301) via the serial control bus. The output of EXPON is input to digital gain control stage VR6.

**VR6** provides a variable gain stage controlled by the microprocessor (U301) over the serial control bus. The gain of the stage may be adjusted in steps of 0.5 dB over the range –1.5 dB to +2.0 dB. The output of VR6 is input to switch **RXMUTE**.

Switch AUDIOLOOPON – DTMFRXON – RXMUTE – EXTRON in conjunction with the summing junction ADD4 allows the microprocessor to control the summation of other audio signals with the receive audio. These addition signals are:

**AUDIOLOOPON** – allows the TX audio from the microphone circuit to be routed to the speaker and **AF_OUT** line.

**DTMFRXON** – allows DTMF tones from the **DTMF GEN** to be routed to the speaker and **AF_OUT** line.

**RXAUION** – allows the receive audio to be routed to the speaker and **AF_OUT** line.

**EXTRON** – allows the **BUZZER** signal, generated by microprocessor (U301) to be routed to the **RINGER_IN** line.

The output of ADD4 is input to Digital Gain Control **VR10**.

VR10 provides a variable gain stage controlled by the microprocessor (U301) over the serial control bus. The gain of the stage may be adjusted in steps of 3 dB over the range –30 dB to +30 dB. The stage provides the user's receive volume control. The output of VR10 is input to amplifier **AMP4**.

**AMP4** provides a unity gain buffer to drive signal line SPEAKER_IN and U401 pin 19 (RECIN). The output of **RECAMP** drives signal line **AF_OUT** that is route to pin 10 of System Connector J104.

7.16 Transmit Audio

An electret microphone is used. DC bias required to power the microphone is derived from the **+3VA** line via R401. C401 provides decoupling of the bias voltage so as to remove noise present on the +3VA supply. Resistor R402 provides the load across which the microphone output voltage is developed. This output voltage is coupled into the **AMP1** (part of U401). Resistors R405 and R404) define the voltage gain of AMP1. The output of **AMP1** is input to switch **MICON**.
Switch MICON is controlled by the microprocessor U301 via the serial control bus. The output of MICON is input to **ADD1/VR1**.
VR1/ADD1 sums the input signals, as selected by switch MICON – EXTINON – DTMFTXON and provides a gain controlled stage controlled from the microprocessor U301 via the serial control bus. The gain of the stage is adjustable over the range – 3.5 dB to +4.0 dB in steps of 0.5 dB. The output of VR1 is routed to U401 pin 59. A bandpass filter within VR1 defines the TX audio speech bandwidth of 300 Hz to 3.4 kHz.
U401 pin 59 is connected to the input pin of **AMP6**, which provides a unity gain amplifier. Resistors R411 and R414 define the voltage gain of the stage. The output of **AMP6** is coupled into U401 pin 58 via capacitor C410. The signal input at U401 pin 58 is routed to the input of digital gain control **ATT1**. The stage gain of **ATT1** is controlled by the microprocessor U301 via the serial control bus. The gain of the stage may be adjusted over the range –22.0 dB to 0.0 dB in steps of 0.5 dB. The output of **ATT1** is input to the compressor stage **COMP**.
The compressor provides amplitude compression of the transmit audio signal such for a 2 dB change in level at the compressor input there is a 1 dB change in level at the compressor output. The compressor may be bypassed by switch **COMPON** under control of the microprocessor U301 via the serial control bus. The output of COMPON is connected to VR2.
**VR2** provides a variable gain stage controlled by the microprocessor (U301) over the serial control bus. The gain of the stage may be adjusted in steps of 0.3 dB over the range –2.1 dB to +2.4 dB. The output of VR2 is input to pre-emphasis and limiter stage **P/E & Limit**.
The **P/E & Limit** stage provides a +6 dB/octave pre-emphasis over the frequency range 300 Hz to 3.4 kHz and includes an amplitude limiter which prevents over deviation of the transmitted carrier. Such deviation limiting is required in order to confine the bandwidth of the transmitted signal to the allocated channel and prevent side bands from spreading into the adjacent channel. The output of the **P/E & Limiter** is input to the **LPF**.
The output of the limiter can contains high order harmonics of the transmit audio signal If not removed these high order harmonics would case the bandwidth of the transmitted signal to be excessive. The Low Pass Filter **LPF**, having a high frequency cut-off at 3.4 kHz removes the high order harmonics. The output of the LPF is input to the Digital Gain Control Stage VR3.
**VR3** provides a variable gain stage controlled by the microprocessor (U301) over the serial control bus. The gain of the stage may be adjusted in steps of 0.3 dB over the range –5.9 dB to +4.8 dB. The output of **VR3** is input to switch **TXAUDON**.
Switch **TXAUDON** is controlled by the microprocessor U301 via the serial control bus. The output of **TXAUDON** is input to **ADD3** Summing Circuit.
**ADD3** sums the transmit audio, the FFSK transmit data stream and the Ø signal as selected by the switch. The output of **ADD3** is input to **VR4**.
**VR4** provides a variable gain stage controlled by the microprocessor (U301) over the serial control bus. The gain of the stage may be adjusted in steps of 0.3 dB over the range –4.5 dB

to +4.8 dB. The output of VR4 is input to SMF1.
Smoothing Filter AMF1 suppresses components of the sampling frequency used within the digital filters of the Base Circuit. These frequency components, if not suppressed, would cause adjacent channel interference to be transmitted.

7.18 EXTIN

Transmit audio signal, derived from the System Connector J104 pin 12, via signal line **AF_IN** is input to U401 pin 63. If the microprocessor (U301) has selected switch **EXTINON**, via the serial control bus, the audio on the **AF_IN** line used to modulate the transmitter. When the microprocessor selects switch **EXTINON** switch **MICON** will be deselected.

7.19 **Ø** -Loop

During call the quality of the connection is monitored by means of the Ø-Signal originated at the Base Station. The tone is at a frequency of 3055, 3985, 4015 or 4045 Hz. The Ø-Signal is received at the MS and is input to the Base Band Circuit together with received audio on signal line **RX-AUDIO**.
The received signal, consisting of both audio and Ø-signal, present at the output of VR5 is routed to the input of **SAT BPF**. **SAT BPF** comprises a band-pass filter having a centre frequency of 4.0 kHz and a pass band of ±55 Hz. The **SAT BPF** removes the audio signal leaving just the Ø-signal. The filtered Ø-signal is input to **VR7**. **VR7** provides a variable gain stage controlled by the microprocessor (U301) over the serial control bus. The gain of the stage may be adjusted in steps of 0.3 dB over the range –4.5 dB to +4.8 dB. The gain setting of the stage controls the deviation of the Ø-signal transmitted by the MS. The output of VR7 is input to switch **FILOOPON**.
If switch **FILOOPON** is selected the Ø-signal is summed with the transmit audio.

7.20 FFSK Demodulation

During certain times signalling and control messages are sent from the BS to the MS. These data messages are transmitted Fast Frequency Shift Keyed (FFSK) with a frequency of 1200 Hz use d to denote logic level 0 and 1800 Hz used to denote logic level 1. The data is transmitted at a bit rat of 1200 bits/sec.
The received signal, consisting containing the FFSK data is input to the BaseBand Circuit via signal line **RX_AUDIO**. At the output of de-emphasis circuit **D/E** the received signal is input the FFSK Demodulator **FFSK DEMOD. The FSSK DEMOD** recovers the serial data together with a clock signal from the incoming FFSK stream. These signals are input to the microprocessor U310 via signal lines **RX_DATA** and **RX_DATA_CLK** respectively.
When a FFSK signal is detected U401 pin 43 **FFSKDET** goes high signifying valid FFSK data. This signal is passed to the microprocessor via signal line **FFSK_DET**.

7.21 FFSK Modulation

Signalling and control messages are sent from the MS to the BS. 1200 bit/sec Fast Frequency Shift Keying (FFSK) is used in order to transmit these messages.
Signal lines **TX_DATA_EN**, **TX_DATA** and **TX_DATA_CLK** are used to transfer data from the microprocessor to the FFSK Modulator contained within U401. In order to initiate data transfer the microprocessor sets the path from the FFSK Modulator to **TX_MOD** by opening the switch **TXAUDON**, to remove speech signals, and then setting the switch **FFSKON.** The processor then sets data line **TX_DAT_EN** high and sends the first data bit. U401 then starts the clock signal **TX_DATA_CLK** that is used by

the microprocessor to control the serial transfer of data to the FFSK Modulator. On the negative edge of **TX_DATA_CLK** the microprocessor places the next bit onto **TX_DATA** line. On the positive edge of **TX_DATA_CLK** the data bit is read into the FFSK Modulator.

7.22 DTMF Encode

The BaseBand circuit U401 contains a Dual Tone Multi Frequency DTMF encoder – **DTMF GEN**. Data written to a register within U401 by the microprocessor U301 via serial bus comprising **/CS_AKM** – **DATA_OUT** – **SCK** – **DATA-IN** controls the sending of DTMF tones.
Before sending DTMF tones the microprocessor U301 signals the BaseBand Circuit U401 to open switch **MICON,** thus removing the speech signal, sets switch **DTMFTXON** on, and then starts DTMF transmission. Once DTMF transmission is complete the microprocessor sets switch MICON on and sets switch DTMFTXON off. Whilst DTMF transmissions are in progress the microprocessor sets switch DTMFRXON allowing DTMF tones to be routed to U401 pin 14 (EXTOUT) and thence to the speaker and the signal line AF_OUT.

7.23 Digital to Analogue Converters

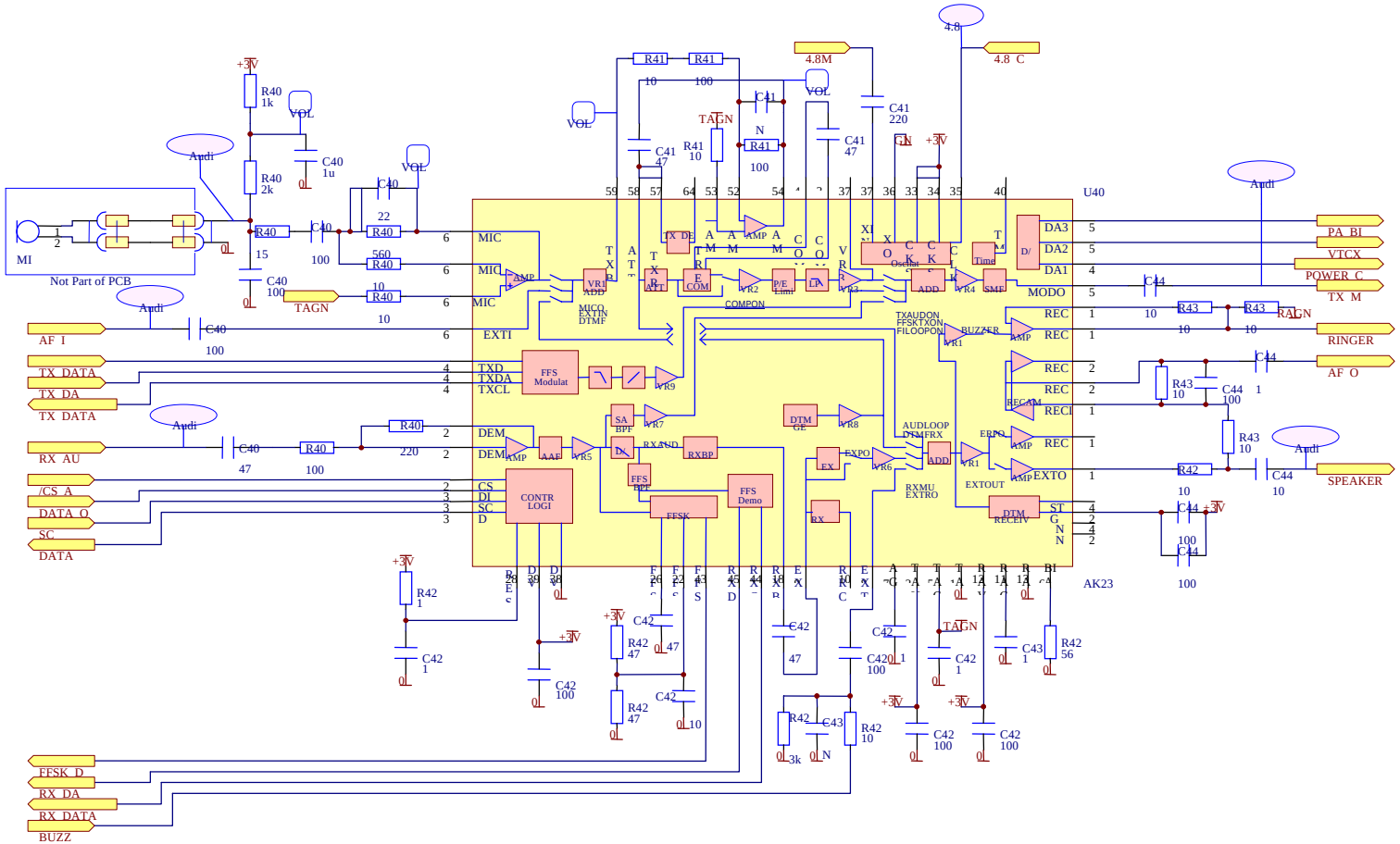
Contained within the BaseBand Circuit U401 are 3 digital to analogue converters **D/A**. The each D/A outputs a dc analogue output level under control of the microprocessor U301 via the serial control bus. These analogue outputs are as follows;
**POWER_CTRL** – Used to control the attenuation of U501 on the transmitter circuit.
**VTCXO** – Used to the tuning of the Voltage Tuned Crystal Oscillator Y601 on the Synthesiser circuit.
**PA_BIAS** – Used to control the gain of U502 and the dc bias current in Q501, both part of the transmitter circuit.

7.24 Oscillator

The **Oscillator** provides various clock signals required within the device. The device is designed to facilitate operation by means of a directly connected quartz crystal of frequency either 14.4 MHz or 4.8 MHz or from and external clock source at a frequency of either 14.4 MHz or 4.8 MHz. The logic level present at pins 36, 33 and 34 configure the device to operate from an external clock source at a frequency of 4.8 MHz. The 4.8 MHz clock source is derived from the Processor circuit via signal line **4.8MHz**.

7.25 Control Logic

Contained within the BaseBand Processor are a number of registers. These registers are used to control the configuration of the BaseBand Processor and provide temporary storage for data to be read out of and written into the device.
The microprocessor U301 communicates with the BaseBand Processor over a serial bus comprising the following data lines:
**/CS_AKM** – When low selects the chip to allow serial transfers to and from the Control Logic.
**DATA_OUT** – Serial data from the microprocessor U301 to the BaseBand Processor.
**SCK –** Serial clock from the microprocessor.
**DATA_IN** – Data from the BaseBand Processor to the microprocessor.




**Circuit Diagram - A66**
**Base-Band Processor**

## Circuit Operational Description - Receiver

7.26 LNA

Q701 operates as a low noise common emitter RF Amplifier. Receive signals, within the allocated NMT450 downlink band, are input to the receiver from the Duplexer part of the transmitter via signal connection **RX_INPUT**.
Power supply to the LNA is derived from the 3VRX line under control of the microprocessor U301. The LNA may be operated at 1 of 2 possible bias points. When **RX_HIGH** is low (approximately 0V) the dc bias point is determined by R703 and R704. These components are designed to set the bias current in Q710 to a low level. When **RX_HIGH** is high an additional path, via R701, D700 and R702, for the flow of base bias current to Q710 is provided. This causes the dc bias current in Q701 to be set to its high level.
The output from Q701 is coupled via impedance matching capacitor C706 to the RF Attenuator.

7.27 RF Attenuator

RF Attenuator comprising resistors R710, R711 and R712 provides a small degree of attenuation of the RX signal, so as to both improve the intermoduation performance of the receiver and provide an impedance match into the RX BPF.

7.28 RF Band Pass Filter

The RF BPF passes the required downlink frequencies and rejects out-of-band signals. The insertion loss of the filter is a maximum of 3 dB over its pass-band.

7.29 1st Mixer

The output impedance of the RX BPF is matched into the gate 2 of the 1st Mixer (Q702) by means of dual L section impedance matching network comprising L710, C720 and L723, C729. The local oscillator injection signal is derived from the RX Synthesiser via signal line **RX_VCO**.
The dc bias point of Q702 is determined by R732.
The drain circuit of Q702 is impedance matched into the 1st IF Filter by means of matching network comprising C733, C732, C734, L712 and C735.

7.30 1st IF Filter

Quartz filter, Y704, having a centre frequency of 45 MHz and a 3 dB bandwidth of 15 kHz defines the channel bandwidth of the receiver 1st IF. The insertion loss of the filter is a maximum of 3 dB over the pass-band. The terminal impedance of the 1st IF Filter is matched to the input impedance of the 1st IF Amplifier by means of impedance matching network comprising L713, C737, L721 and C748.

7.31 1st IF Amplifier

Cascade connected bipolar transistors Q703 and Q704 provide approximately 20 dB of voltage gain at the 1st IF frequency.
Impedance matching network comprising C747 and L720 provides

matching into the 2nd Mixer stage Input, U701 Pin 32, via C740.

7.32 2nd LO X3 Freq Multiplier

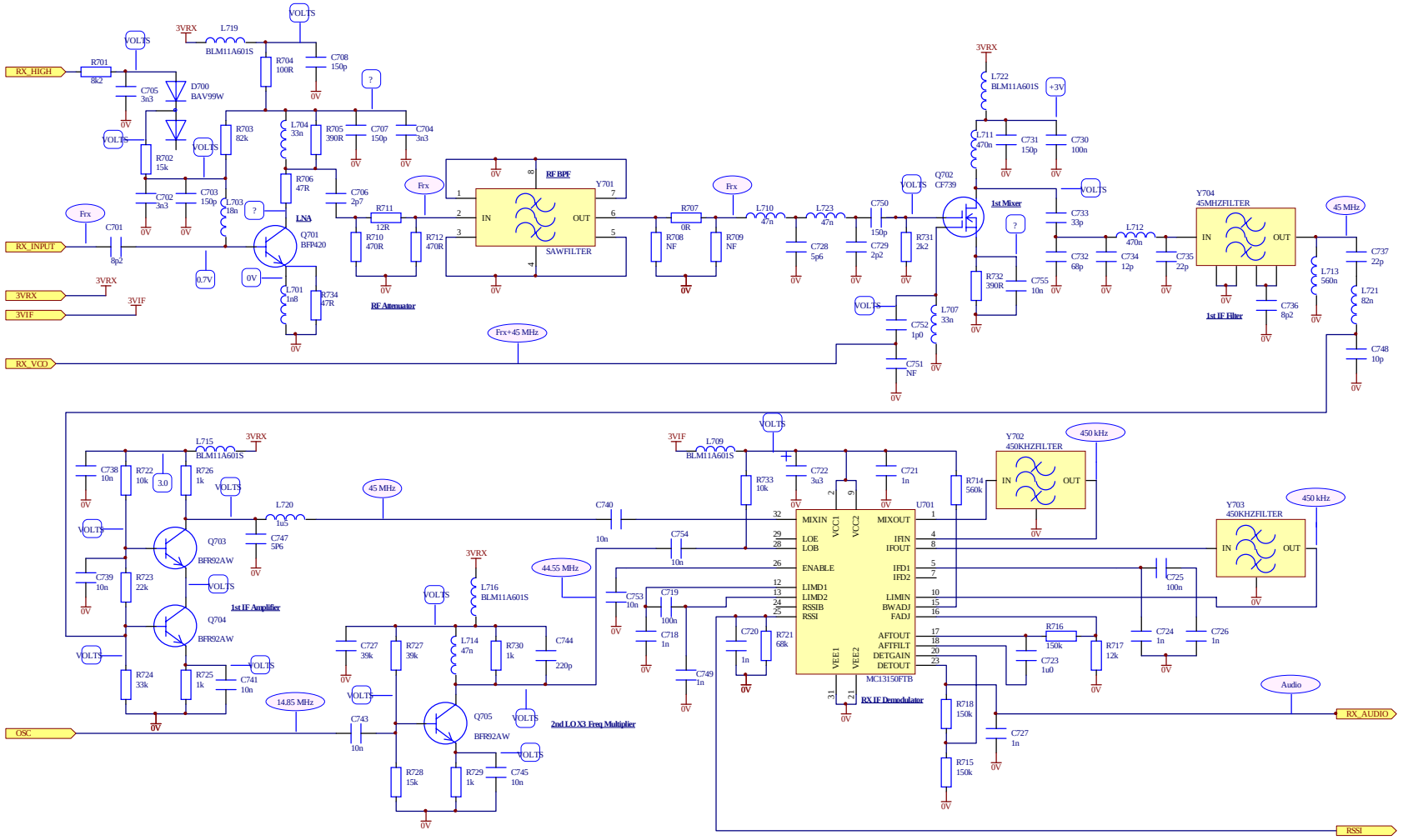
The output frequency, 14.85 MHz, of the VCTCXO, connected by signal line **OSC,** is frequency multiplied by Q705. The collector circuit of Q705, comprising a parallel resonant circuit, is tuned to 44.55 MHz. Thus the 3rd harmonic of the VCTCXO frequency is generated.

7.33 RX IF Demodulator

The output of the 1st IF Amplifier is coupled into the 2nd Mixer via C754. The 2nd Local Oscillator injection frequency of 44.55 MHz is coupled into U701 by means of C754.
The components of the output spectrum of the 2nd Mixer (U701 pin 1) occurring at the 2nd IF frequency of 450 kHz are selected by BPF Y702 which has a centre frequency of 450 kHz.
The output of Y702 feeds the input to the 2nd IF Amplifier contained within U701 via U701 pin 4. The output 2nd IF Amplifier feeds the input of BPF Y703, also having a centre frequency of 450 kHz, providing further selectivity at the 2nd IF frequency. The output of Y703 is feed to the input of the $2^{nd}$ IF Limiter Stage contained within U701. The limiter stage limits the amplitude of the received signal presented to the Demodulator thus providing suppression of amplitude modulated signals FM signal /noise improvement.
The output of the Limiter is coupled into the Demodulator.
The Demodulator converts the incoming modulated carrier to audio baseband. The audio signal is output to the BaseBand Processor via signal line **RX_AUDIO**.

7.34 RSSI

U701 provides a Receive Signal Strength Indicator RSSI (U701 pin 25). The dc signal level on the RSSI line is approximately proportional to the logarithm of the received signal level. The RSSI signal is input to the microprocessor via signal line **RSSI**.




## Circuit Diagram - A66
## Receiver

## Circuit Operational Description - Synthesiser

7.35 Reference Oscillator

Y601 Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO) provides the reference frequency used to determine both the TX and the RX frequencies. The oscillator produces a highly accurate output frequency of 14.85 MHz.
The output frequency of the reference oscillator can be adjusted, over a frequency range of ±7 ppm (parts per million) i.e. ±104 Hz. by the voltage present on signal line **VCTCXO**. The voltage level on signal line **VCTCXO is** derived from the output of **D/A DA20** located on the BaseBand Circuit.
During the calibration of the phone the voltage present on signal line **VCTCXO** is adjusted so as to reduce the error of the TX carrier frequency to less than ±5 Hz. The calibration value corresponding to this error is written to the phone's EEPROM memory. When the phone is in operation the microprocessor writes the calibration value to **D/A DA20**, which outputs the correct voltage level on signal line **VCTCXO** so as to tune out the frequency error of the Reference Oscillator.
The output of the Reference Oscillator is input to the reference input of the Dual PLL Synthesiser U601 at pin 6. The output of the Reference Oscillator is also fed 2nd LO X3 Frequency Multiplier stage, located on the Receiver Circuit, where it is used to derive the injection frequency for the Receiver 2nd Mixer.

7.36 TX Synthesiser

The TX Synthesiser comprises a feedback system. The output of the **TX VCO** Y602 is fed back into the input of **Dual PLL Synthesiser** chip U601 at pin 5. Within U601 the TX VCO frequency is divided down by the preset ratio of the two stage RF divider chain comprising a dual modulus prescaler (P) and a divide by N counter (N). The P and N counters are programmable from the microprocessor over the serial control lines **SCK**, **DAT_OUT** and **SYNTH_LOAD**. Thus the microprocessor can set the division ration of the RF divider chain.
The 14.85 MHz reference frequency, derived from Y601, is input to U601 pin 6 (OSCIN). Within U601 OSCIN feeds the input to a programmable divider (R) which divides the reference frequency. The R counter is programmed by the microprocessor over the serial control lines **SCK**, **DAT_OUT** and **SYNTH_LOAD**. Thus the microprocessor can set the division ration of the Reference Frequency divider chain.
The output of N and the output of P are input to the two inputs of a phase detector contained within U601. The phase detector produces an output current presented at U601 pin 3 (DO1) which represents the phase error between the TX VCO frequency, and the Reference Frequency.
The output of the phase detector is input to the TX VCO Y602 control pin (CTRV) via the **TX Loop Filter** comprising C607, C608 C617, R604, R605 and C610. The Loop filter converts the output current of the synthesiser to a voltage that is input to the TX CO.
The TX VCO produces an output frequency that is a function of the control voltage present at CTRV. The polarity of the control voltage produced by the phase detector is such as to adjust the VCO to reduce the phase error between the two inputs to the phase detector to zero. When this occurs the Phase Lock Loop attains phase lock and the percentage frequency accuracy of the TX is equal

to the percentage frequency accuracy of the reference frequency.
The output of **TX VCO** present at Y602 OUT is attenuated by resistors R607, R608 and R609 and drives the transmitter via signal line **TX_VCO**.

7.37 Transmitter Modulation

The **TX VCO** Y602 provides modulation input, **MOD**. Transmit audio, derived from the BaseBand Processor, is input via signal line **TX_MOD**. Audio signals present on **MOD** frequency modulate the **TX VCO** frequency thus producing frequency modulation of the transmitted carrier.

7.38 RX Synthesiser

The RX Synthesiser comprises a feedback system similar but separate to the TX Synthesiser. The output of the **RX VCO** Y603 is fed back into the input of **Dual PLL Synthesiser** chip U601 at pin 12. Within U601 the **RX VCO** frequency is divided down by the preset ratio of the two stage RF divider chain comprising a dual modulus prescaler (P) and a divide by N counter (N). The P and N counters are programmable from the microprocessor over the serial control lines **SCK**, **DAT_OUT** and **SYNTH_LOAD**. Thus the microprocessor can set the division ration of the RF divider chain.

The 14.85 MHz reference frequency, derived from Y601, is input to U601 pin 6 (**OSCIN**). Within U601 **OSCIN** feeds the input to a programmable divider (R) which divides the reference frequency. The R counter is programmed by the microprocessor over the serial control lines **SCK**, **DAT_OUT** and **SYNTH_LOAD**. Thus the microprocessor can set the division ratio of the Reference Frequency divider chain.
The output of N and the output of P are input to the two inputs of a phase detector contained within U601. The phase detector produces an output current presented at U601 pin 14 (**DO2**) which represents the phase error between the RX VCO frequency, and the Reference Frequency.
The output of the phase detector is input to the **RX VCO** Y603 control pin (**CTRV**) via the **RX Loop Filter** comprising C612, C613, R611, R612, and C615. The Loop filter converts the output current of the synthesiser to a voltage that is input to the TX CO.
The **RX VCO** produces an output frequency that is a function of the control voltage present at **CTRV**. The polarity of the control voltage produced by the phase detector is such as to reduce the phase error between the two inputs to the phase detector to zero. When this occurs the Phase Lock Loop achieves phase lock and the percentage frequency accuracy of the TX is equal to the percentage frequency accuracy of the reference frequency.
The output of **RX VCO** present at Y603 OUT is attenuated by resistors R614, R615 and R616 and drives the local oscillator injection into the Receiver 1st Mixer via signal line **RX_VCO**.

7.39 VTX Regulator

**VTX** Regulator comprising U602 provides a regulated supply of +3 V to power the low-level stages of the transmitter and the **TXVCO**. A supply of nominal voltage +3.3 V is input via line +B from the Power Circuit. The regulator is enabled by signal line **3V_TX_EN** derived from the microprocessor U301.

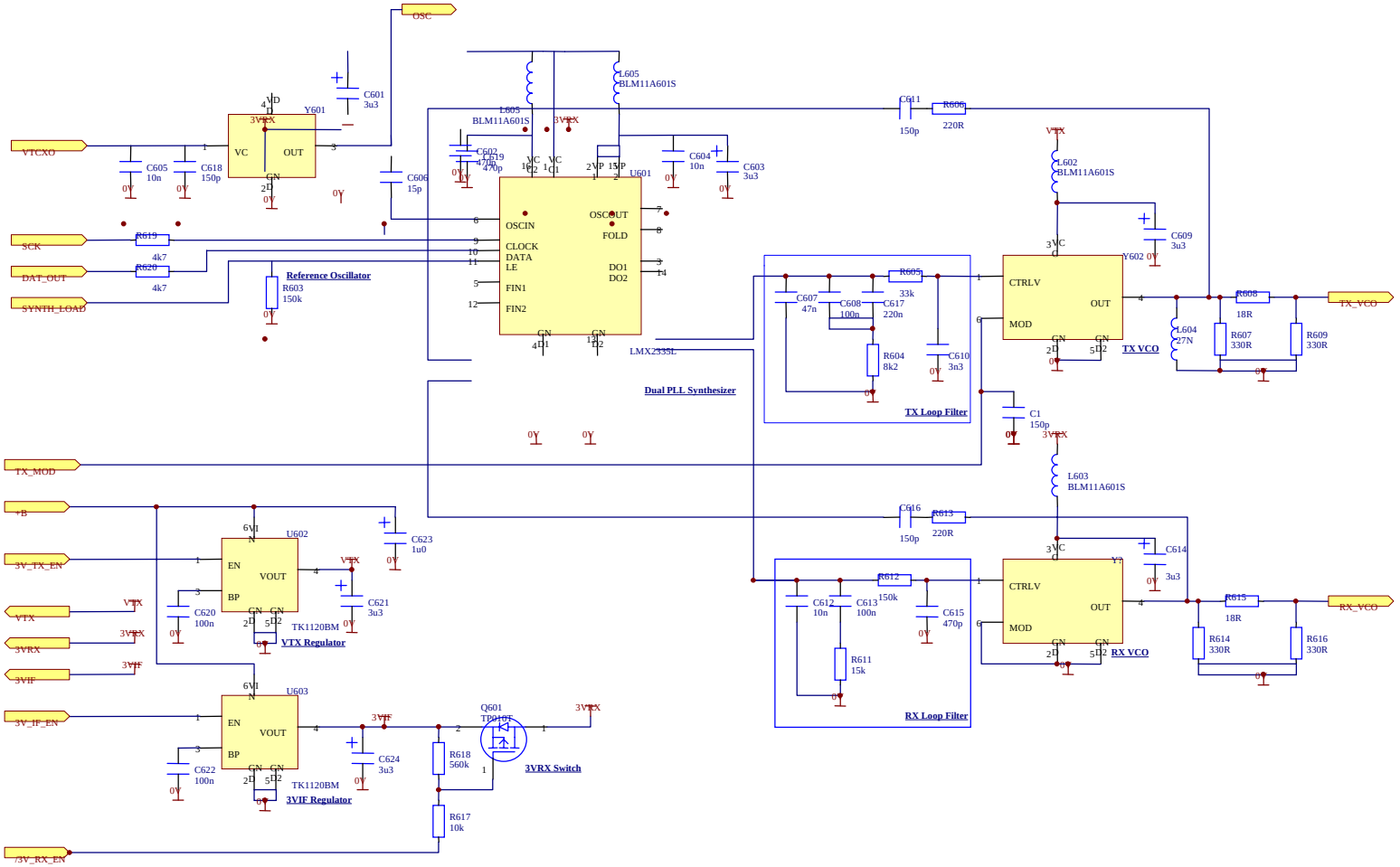
7.40 3VIF Regulator

**3VIF** regulator comprising U603 provides a regulated supply of +3 V to power the IF stages of the receiver. Its input supply is derived from the **+B** line from the Power Circuit. The regulator is enabled by signal line **3V_IF _EN** derived from the microprocessor U301.

7.41 3VRX Switch

**3VRX** Switch comprising transistor Q601 switches the +3V output of the **3VIF** regulator to the **LNA**, **1st Mixer, 2nd IF Amplifier, 2nd LO X3Freq Multiplier** stages of the receiver and

the **RXVCO** via the **3VRX** line. The switch is control by the microprocessor U301 via control line **/3V_RX_EN**.




## Circuit Diagram - Synthesiser

## Circuit Operational Description - Transmitter

### 7.42 Attenuator

The attenuator stage U501 provides electronically adjustable attenuation under the control of the microprocessor via analogue signal line **POWER_CTRL.** The **TX** carrier frequency, generated by the TX Synthesiser is input to this stage, via signal line **TX_VCO**, at an approximate level of – 6 dBm. The minimum attenuation of the stage is 2.7 dB for a **POWER_CTRL** voltage of +3 V.
The output of the Attenuator Stage is coupled to the Gain Controlled Amplifier via C503.

### 7.43 Gain Controlled Amplifier

The power gain of this stage is controlled by the microprocessor, U301; via the signal line PA-BIAS buffered by the Unity Gain Buffer (U503). The voltage on the PA_BIAS control line controls the gain of the stage. During calibration the gain of the stage is adjusted so as to set the TX power delivered to the Antenna to 100 mW.
The output of the Gain Controlled Amplifier (U502 pin 1) is coupled to the **TX Interstage Band Pass Filter** by means of C506.

### 7.44 TX Interstage Band Pass Filter

The TX Interstage BPF (Y501) provides attenuation of the noise sidebands of the TX VCO occurring within the RX downlink band. Its insertion loss, within the uplink band of frequencies is a maximum of 3 dB.

### 7.45 TX Power Amplifier

The TX Power Amplifier provides power gain to raise the level of the transmitter output to 200 mW, which, after the loss in BPFTX of 3 dB, produces a nominal 100 mW at the antenna. The dc bias point of the stage is set by the voltage level present on control line PA_BIAS under control of the microprocessor U301. When transmit operation is not required, i.e. during stand-by, the PA_BIAS line is low thus turning off the dc bias to the TX Power Amplifier. This ensures that the power consumption of the TX, during stand-by is minimised.
The collector supply to Q501 is derived directly from the battery pack output via line **+B**.
The output of Q501 is coupled to the input of **BPF_TX** (Y503) via impedance transforming network comprising C516, L500 and C515.

### 7.46 Duplexer

The Duplexer comprises the TX Band Pass Filter and the RX Band Pass Filter. The Duplexer is required in order to allow the use of a common antenna for both TX and RX. Signals originating from the TX are passed through the BPF-TX with an attenuation of less than 3 dB. When TX signals reach the junction point comprising C518, L507 they are presented with impedance of the order of 50 ς in the direction of the antenna, but much higher impedance in the direction of the receiver i.e. via L707. Thus the majority of the TX power is directed into the antenna. Receive signals arriving at the antenna, are conducted to the junction of C518 and L507. These signals see high impedance in the direction of the TX Band Pass Filter but impedance of approximately 50 ς in the direction of the RX Band Pass Filter. Signals, within the downlink frequency band, pass through the RX Band Pass Filter with an attenuation of less than 3 dB.

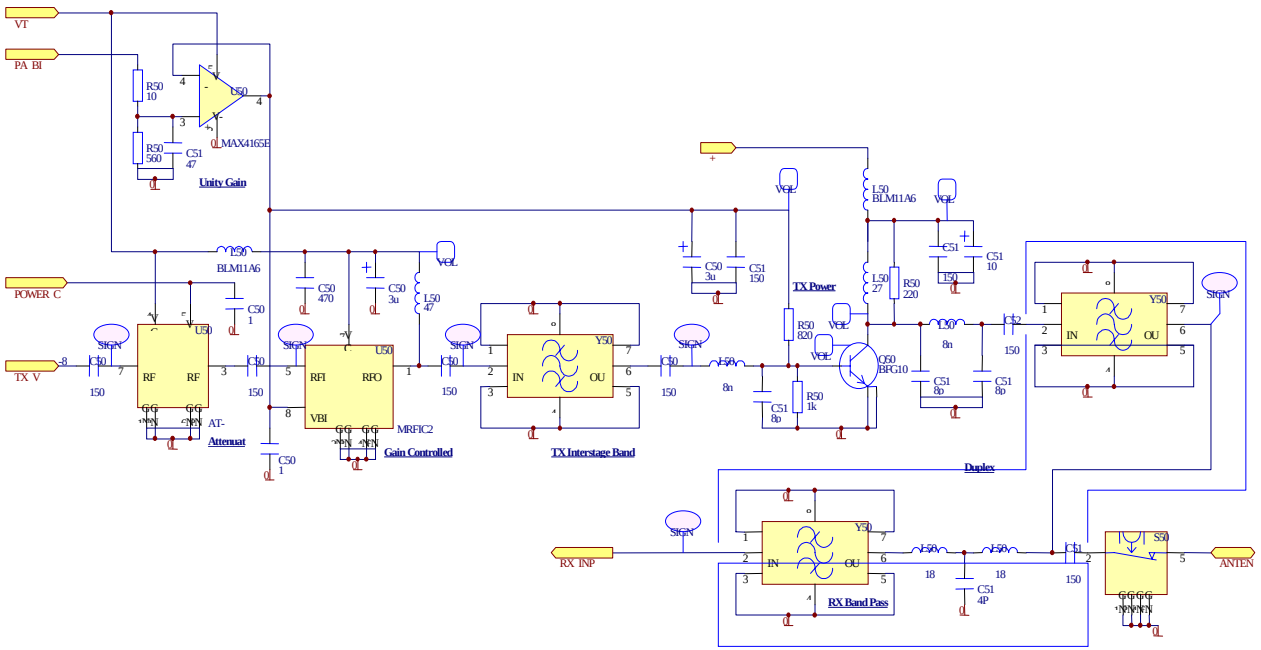
### 7.47 External Antenna Socket

When no external antenna is connected the External Antenna Socket S501 provides a direct path to

The integral antenna fitted to the top of the phone. When an external antenna is connected a switch within the External Antenna Socket disconnects the phone's set top antenna and connects the external antenna.

7.48 Unity Gain Buffer

The Unity Gain Buffer provides a non-inverting voltage gain of X1 and allows the output of the Digital to Analogue Converter (DA10), located within U401 on the BaseBand circuit, to control the level of bias current in the TX Power Amplifier via control line **PA_BIAS**.




**Circuit Diagram - A66**
**Transmitter**

# 8 Calibration Procedure

***Note: Calibration is required following the replacement of any electrical component. Ensure that the PCB Assembly is fitted within the plastic case and that the fixings screws are tightened to the specified torque***

8.1 Equipment Required

| Item | Description | Tellit P/n | Qty | Remarks |
|---|---|---|---|---|
| 1 | IBM Compatible PC with Pentium 100 or higher, fitted with 32 MB RAM and CD ROM Drive and Mouse | | 1 | |
| 2* | Cable Assembly 9W D Plug – 9W D Socket | xxxxx | 1 | |
| 3* | Cable Assembly 25W D Plug – 25W D Socket | xxxxx | 1 | |
| 4* | Mains Charger or PSU set to 6V 600mA max | xxxxx | 1 | |
| 5 | RF Communications Test Set | | 1 | HP 8920B or similar |
| 6* | Cable Assembly 50Ω BNC Plug - 50Ω BNC Plug | | 3 | |
| 7 | Power Supply Unit 12 V dc Hum & Noise < 50 mV pp | | 1 | |
| 8* | Test Interface Box A66/A77 | | 1 | |
| 9* | Cable Assembly 37W D Plug to 37W D Plug | | 1 | |
| 10* | Test Fixture A66 Phone | | 1 | |
| 11 | Coaxial Adapter SMA Socket – N Plug | | 1 | |
| 12 | Coaxial Lead Assembly 50Ω BNC Plug - 50Ω BNC Plug | | 1 | |
| 13 | Digital Multimeter | | 2 | |
| 14* | Test Lead 4mm Plug – 4mm Plug Red | xxxxx | 3 | |
| 15* | Test Lead 4mm Plug – 4mm Plug Black | xxxxx | 3 | |

8.2 Connecting the Equipment

8.2.1 Connect the equipment as shown in Figure 8-1 below.

8.3 Starting up the Diagnostics Software

8.3.1 Start the Tellit Service and Diagnostic Software by clicking the icon. The TELLIT logo screen is displayed. Click on “CLICK TO CONTINUE”.

8.4 Get Phone Details

8.4.1 The Get Phone Details window is displayed. Select the appropriate frequency band corresponding to the band of the phone to be calibrated, e.g. Band 1, by checking the required band option.

8.4.2 The transmit and receive radio frequencies corresponding to the selected band, together with a list of countries, are displayed.

8.4.3 Select the model of the phone to be calibrated by checking the required model option.

8.4.4 The version of the software in the phone is automatically displayed in the text window.

8.4.5 Once frequency band and phone type have been selected click “OK” to proceed.

8.5 Main Menu

8.5.1 Click the “CALIBRATE” button to proceed to the Calibration Menu.

8.6 Calibration Menu

***Note: When calibrating the phone ensure that all calibration functions are performed in the order in which the calibration function buttons are presented. Start at TX Freq and finish at SAT Dev ensuring that all calibrations are performed.***

8.7 TX Frequency

8.7.1 Click “TX FREQ”.

8.7.2 Read the upper text area of the window to receive guidance on the calibration procedure.

8.7.3 Measure the transmitter frequency using the RF Communication Test Set (the mobile terminal’s transmitter is automatically keyed on).

8.7.4 Adjust the “SET TX FREQUENCY” slider at the bottom of the window until the transmitter frequency displayed on the RF Communication Test Set corresponds as near as possible to the frequency value shown in the text box. This can be done by repeatedly clicking the left or right arrows on either side of the slider or by continuously left-clicking the slider control and dragging it across its range.

8.7.5 When satisfied with the frequency value, click on the “SAVE CAL” button to store the calibration value.

8.7.6 Click the “QUIT” button to return to the calibration menu.

8.8 RX RSSI

8.8.1 Click “RX RSSI”.

8.8.2 Read the instructions shown in the text box.

8.8.3 Adjust the RF Communication Test set to produce an unmodulated RF output at a level of +20 dBμV 1 with the frequency requested on the PC display.

8.8.4 Click the “SAVE CAL” button to store the calibration value.

8.8.5 Increment the RF level in steps of +10 dB up to +70 dB clicking the “UPDATE” button after each step, verifying that the displayed RF level in the window is correct to within the tolerance as stated within the text window.

8.8.6 Click the “QUIT” button to return to the calibration menu.

8.9 TX Power

8.9.1 Click “TX POWER”.

8.9.2 Refer to the instructions shown in the text box.

8.9.3 Measure the TX Power using the RF Communications Test Set.

8.9.4 If necessary, adjust the “SET TX POWER” slider to obtain and output as stated within the text window.

8.9.5 Click the “SAVE CAL” button to store the calibration value.

8.9.6 Click the “QUIT” button to return to the calibration menu.

8.10 RX Audio Level

8.10.1 Click “RX AUDIO LEVEL”.

8.10.2 Read the upper text area of the window to receive guidance on the calibration procedure.

8.10.3 Set up the RF Communications Test Set to output a signal as instructed with the frequency, level and modulation requested.

8.10.4 Adjust the “SET RX AUDIO LEVEL” slider at the bottom of the window until the audio output level displayed on the RF Communications Test Set corresponds as near as possible to the value shown in the text box. This can be done by repeatedly clicking the left or right arrows on either side of the slider or by continuously left-clicking the slider control and dragging it across its range.

8.10.5 Click the “SAVE CAL” button to store the calibration value.

8.10.6 Click the “QUIT” button to return to the calibration menu.

8.11 TX Max Deviation

8.11.1 Click “TX MAX DEV”.

8.11.2 Following the on-screen instructions, set the audio signal (from the RF Communications Test Set to TXAF_IN of the mobile terminal) to the values stated in the text box on the PC screen. Ensure that the RF Communications Test Set filters and detector settings are as instructed. Measure the frequency deviation as stated ensuring the filters in the RF Communications Test Set are set correctly.

8.11.3 Adjust the “SET MAX TX DEVIATION” slider at the bottom of the window until the frequency deviation displayed on the RF Communications Test Set corresponds as near as possible to the target value shown in the text box. This can be done by repeatedly clicking the left or right arrows on either side of the slider or by continuously left-clicking the slider control and dragging it across its range.

8.11.4 Click the “SAVE CAL” button to save the calibration value.

8.11.5 Click the “QUIT” button to return to the calibration menu.

8.12 TX Audio Deviation

8.12.1 Click “TX AUDIO DEVIATION”.

8.12.2 Following the on-screen instructions, connect the stated audio source to AF IN of the mobile terminal. Measure the frequency deviation as stated ensuring the filters in the RF Communications Test Set are set correctly.

8.12.3 Adjust the “SET TX NORMAL DEVIATION” slider at the bottom of the window until the frequency deviation displayed on the RF Communications Test Set corresponds as near as possible to the target value shown in the text box. This can be done by repeatedly clicking the left or right arrows on either side of the slider or by continuously left-clicking the slider control and dragging it across its range.

8.12.4 Click the “SAVE CAL” button to store the calibration value.

8.12.5 Click the “QUIT” button to return to the calibration menu.

8.13 FFSK Deviation

8.13.1 Click “FFSK DEV”.

8.13.2 Following the on-screen instructions, measure the frequency deviation using the RF Communications Test Set. Ensure that the filter values and deviation units stated in the text box are set on the RF Communications Test Set.

8.13.3 Adjust the “SET TX FFSK LEVEL” slider at the bottom of the window until the frequency deviation displayed on the RF Communications Test Set corresponds as near as possible to the target value shown in the text box. This can be done by repeatedly clicking the left or right arrows on either side of the slider or by continuously left-clicking the slider control and dragging it across its range.

8.13.4 Click the “SAVE CAL” button to store the calibration values.

8.13.5 Click the “QUIT” button to return to the calibration menu.

8.14 SAT Dev

8.14.1 Click “SAT DEV”.

8.14.2 Read the upper text area of the window to receive guidance on the calibration procedure. Set up the RF Communications Test Set as instructed.

8.14.3 Inject a RF signal with a level, frequency and deviation as stated in the text box. Measure the frequency deviation of the transmitter using the RF Communications Test Set to the filter values stated in the text box.

8.14.4 Adjust the “SET SAT DEVIATION” slider at the bottom of the window until the frequency deviation displayed on the RF Communications Test Set corresponds as near as possible to the target value shown in the text box. This can be done by repeatedly clicking the left or right arrows on either side of the slider or by continuously left-clicking the slider control and dragging it across its range.

8.14.5 Click the “SAVE CAL” button to store the calibration value.

8.14.6 Click the “QUIT” button to return to the calibration menu.

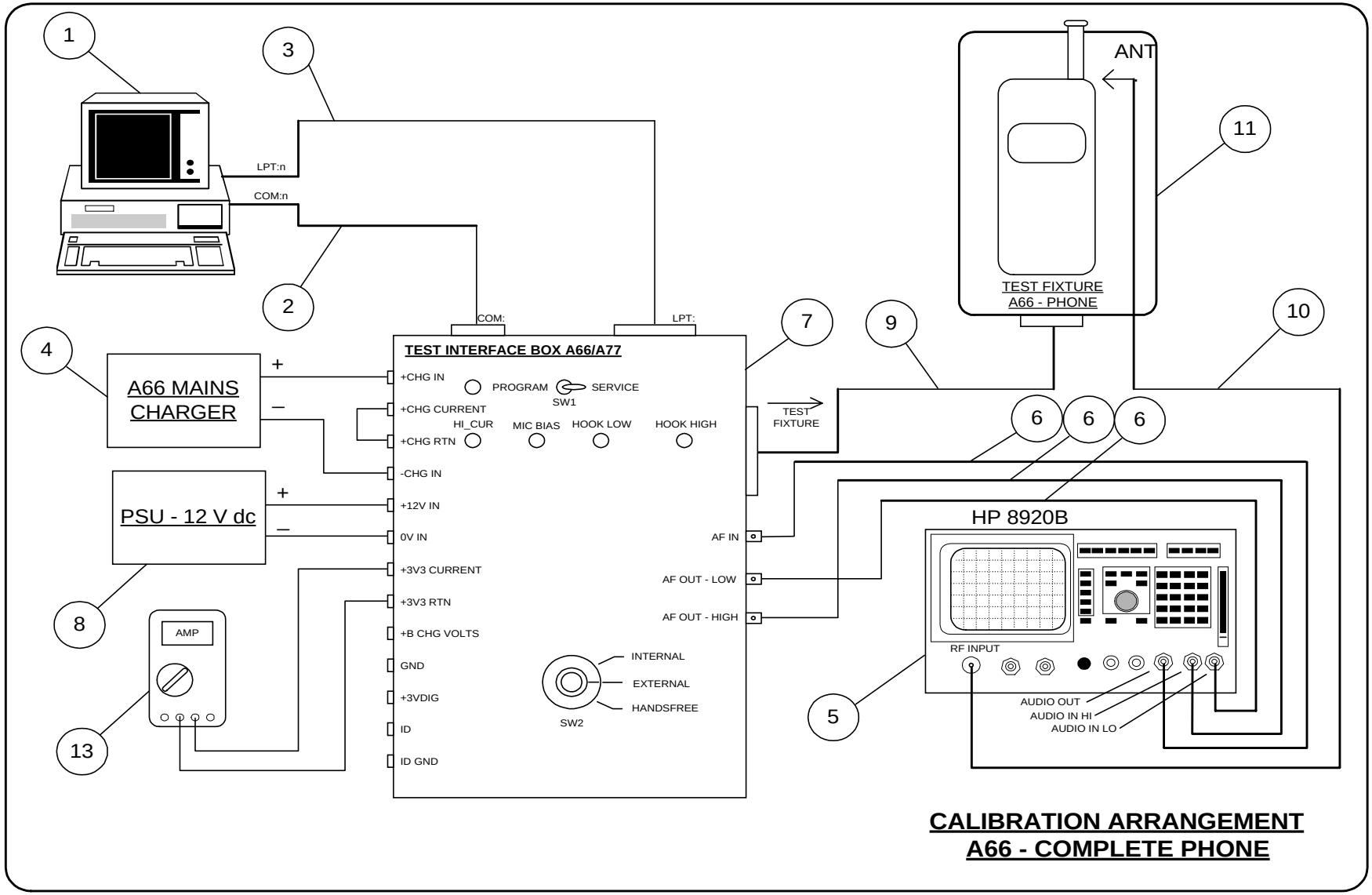

1
3
LPT:n
COM:n
2
ANT
11
TEST FIXTURE
A66 - PHONE
10
COM:
LPT:
7
9
4
A66 MAINS
CHARGER
+
–
TEST INTERFACE BOX A66/A77
+CHG IN
PROGRAM
SERVICE
SW1
+CHG CURRENT
HI_CUR
MIC BIAS
HOOK LOW
HOOK HIGH
+CHG RTN
TEST
FIXTURE
6
6
6
-CHG IN
PSU - 12 V dc
+
–
+12V IN
0V IN
HP 8920B
AF IN
+3V3 CURRENT
AF OUT - LOW
+3V3 RTN
AF OUT - HIGH
8
AMP
+B CHG VOLTS
RF INPUT
GND
INTERNAL
EXTERNAL
HANDSFREE
+3VDIG
SW2
ID
AUDIO OUT
AUDIO IN HI
AUDIO IN LO
5
13
ID GND
CALIBRATION ARRANGEMENT
A66 - COMPLETE PHONE

Figure 8-1

# 9 Programming Procedure

***Note: Programming of the phone is required following the replacement of the main processor (U301) or the external EEPROM (U302). If either of these devices have been changed the phone must be programmed before any other testing can be conducted. Programming may be performed with the PCB contained within the case or alternatively, if required, with the PCB removed from the case.***

***Note: Failure of the main processor, failure of the external EEPROM or programming the phone will erase the contents of the phone book. Before changing either of these devices or programming the phone attempt to save the contents of the phone book using the configuration tool Forte.***

***Note: Programming the phone will result in the loss of the calibration values stored in the internal EEPROM.***

***Following programming you must recalibrate the phone.***

9.1 Equipment Required

| Item | Description | Tellit P/n | Qty | Remarks |
|---|---|---|---|---|
| 1 | IBM Compatible PC with Pentium 100 or higher fitted with 32 MB RAM and CD ROM Drive and Mouse | | 1 | |
| 2* | Cable Assembly 9W D Plug – 9W D Socket | xxxxx | 1 | |
| 3* | Cable Assembly 25W D Plug – 25W D Socket | xxxxx | 1 | |
| 4* | Mains Charger | xxxxx | | |
| | | | | |
| | | | | |
| 7 | Power Supply Unit 12 V dc Hum & Noise < 50 mV pp | | 1 | |
| 8* | Test Interface Box A66/A77 | xxxxx | 1 | |
| 9* | Cable Assembly 37W D Plug to 37W D Plug | xxxxx | 1 | |
| 10* | Test Fixture A66 Phone | xxxxx | 1 | |
| 11* | Test Fixture A66 PCB | xxxxx | 1 | |
| | | | | |
| | | | | |
| 14 | Digital Multimeter | | 2 | |
| 15* | Test Lead 4mm Plug – 4mm Plug Red | xxxxx | 3 | |
| 16* | Test Lead 4mm Plug – 4mm Plug Black | xxxxx | 3 | |
| | | | | |

9.2 Connecting the Equipment

9.2.1 Connect the equipment as shown in Figure 9-1 below.

9.3 Starting up the Diagnostics Software

9.3.1 Start the Tellit Service and Diagnostic software by clicking the icon. The TELLIT logo screen is displayed. Click on “CLICK TO CONTINUE”.

9.4 Get Phone Details

9.4.1 The Get Phone Details window is displayed. Select the appropriate frequency band corresponding to the band of the phone to be programmed, e.g. Band 1, by checking the required band option.

9.4.2 The transmit and receive radio frequencies corresponding to the selected band, with a list of countries, are displayed.

9.4.3 Select the model of phone to be programmed by checking the required model option.

9.4.4 The version of the software in the phone is automatically displayed in the text window.

9.4.5 Once frequency band and phone type has been selected; click “OK” to proceed.

9.5 Main Menu

9.5.1 Click the “PROGRAM” button to launch the Atmel ISP programming utility.

9.5.2 Follow the onscreen instructions to set switch SW [RDL2] on the Test Interface Box to position “PROGRAM”.

9.6 Programming

9.6.1 From the Atmel AVR ISP menu bar choose Project – Open Project or alternatively choose the Open Project tool on the tool bar.

9.6.2 From the pop-up Option [RDL1] Box navigate to the programming project file e.g. A66_276.avr.

***Note: The file naming convention used for programming project files is as follows:***

***Example – A66_276.avr***
***: :……Software Version***
***:……Phone Model***

Double click the file to open it.

9.6.3 From the menu bar choose Program – Program Device. Observe the progress bar as the programming of the device proceeds.

9.6.4 When the message box “Program Complete – No errors” appears click the “OK” button.

9.6.5 Click on the right hand top of screen to close program function.

9.6.6 Follow the onscreen instructions to set switch SW [RDL2] on the Test Interface Box to position “SYSTEM”.

***Note: Following programming perform calibration and test of the phone.***

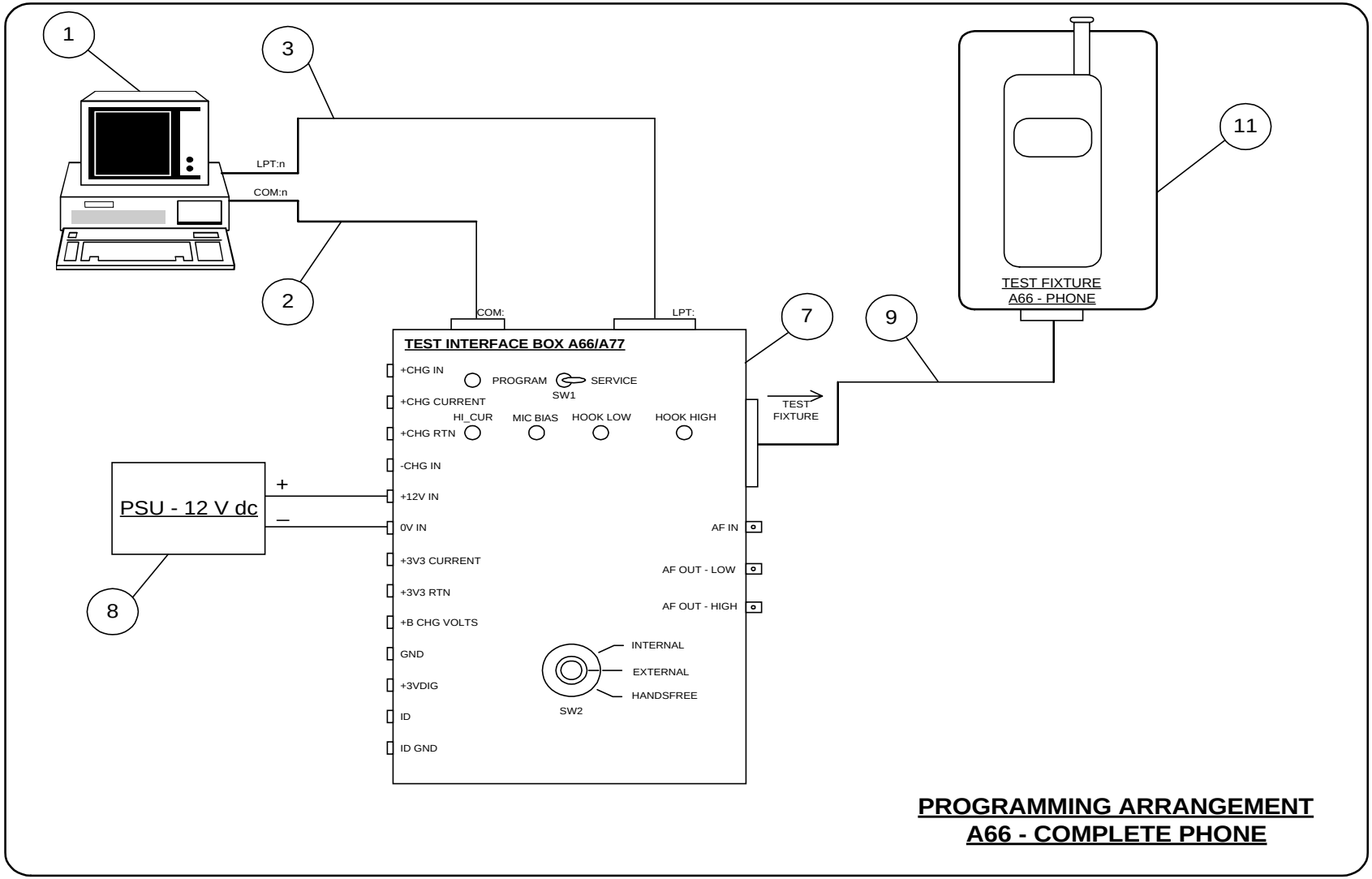

1
3
LPT:n
COM:n
2
COM:
LPT:
TEST INTERFACE BOX A66/A77
+CHG IN
PROGRAM
SERVICE
SW1
+CHG CURRENT
HI_CUR
MIC BIAS
HOOK LOW
HOOK HIGH
+CHG RTN
-CHG IN
+12V IN
0V IN
+3V3 CURRENT
+3V3 RTN
+B CHG VOLTS
GND
+3VDIG
ID
ID GND
AF IN
AF OUT - LOW
AF OUT - HIGH
INTERNAL
EXTERNAL
HANDSFREE
SW2
PSU - 12 V dc
+
–
8
7
9
TEST
FIXTURE
TEST FIXTURE
A66 - PHONE
11
PROGRAMMING ARRANGEMENT
A66 - COMPLETE PHONE

Figure 9-1

# 10 Basic Servicing Procedure - 2

10.1 Removing the Battery Pack

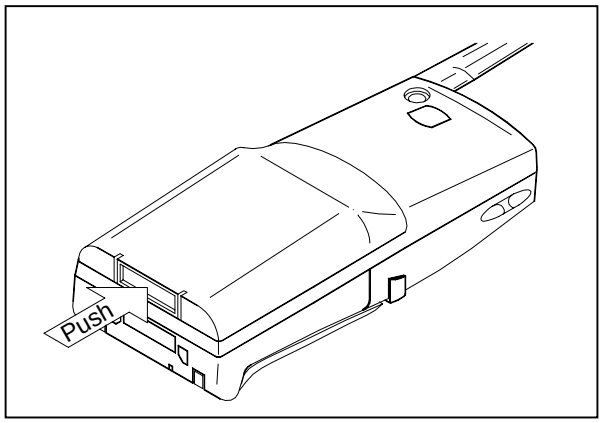



Figure 10-1

10.1.1 Push the Battery Release Catch as shown in Figure 10-1 above.

10.1.2 Lift the Battery Pack off the phone.

10.2 Removing the Volume Button

10.2.1 Lever out the Volume Button using a small Jeweller's screwdriver inserted into the position on the volume button as shown in Figure 10-2.

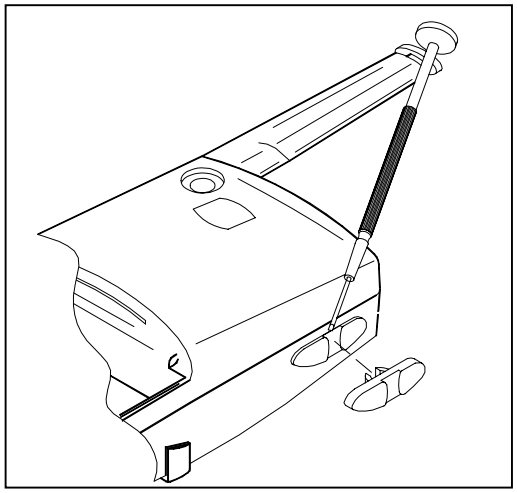


Figure 10-2

***Caution – Take care not to damage the plastic case of the phone.***

10.3 Removing the Back Moulding

10.3.1 Remove the volume button as described in 10.2 above.

10.3.2 Remove the Clip Hole Mould using a small Jeweller's screwdriver as described in Figure 10.3 below.

10.3.3 Unscrew 4 screws using a small Torx™ screwdriver size T6 X 60 and retain screws.

10.3.4 Carefully lift off the back moulding.

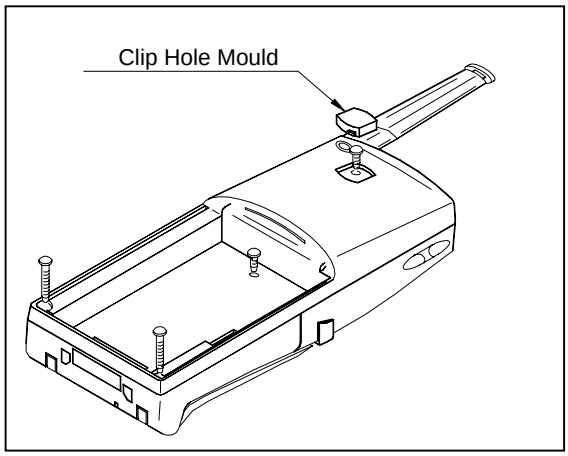



Figure 10-3

10.4 Removing the PCB

10.4.1 Remove the volume button as described in 10.2 above.

10.4.2 Remove the back moulding as described in 10.3 above.

10.4.3 Hinge the PCB up and remove screw and distance sleeve as shown in Figure 10-4 below. Retain the screw and distance sleeve.

10.4.4 Lift the PCB assembly out taking care not to damage the antenna contact.

10.4.5 Store the PCB assembly in an anti-static bag.

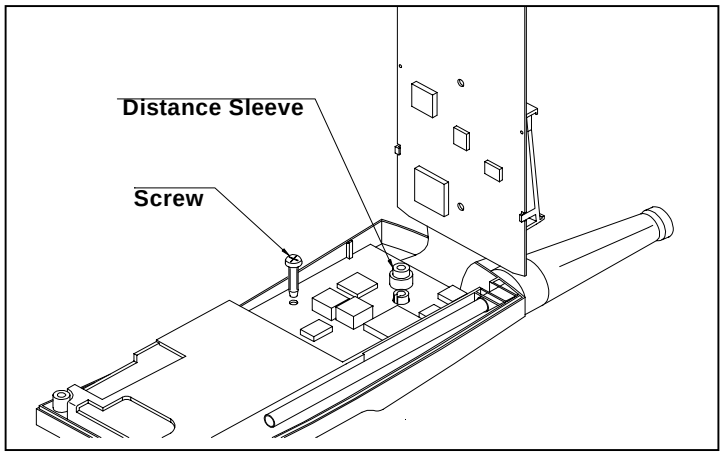



Figure 10-4

10.5 Changing the Cover Moulding

10.5.1 Squeeze the sides of the cover moulding as shown in Figure 10-5 below and lift out.

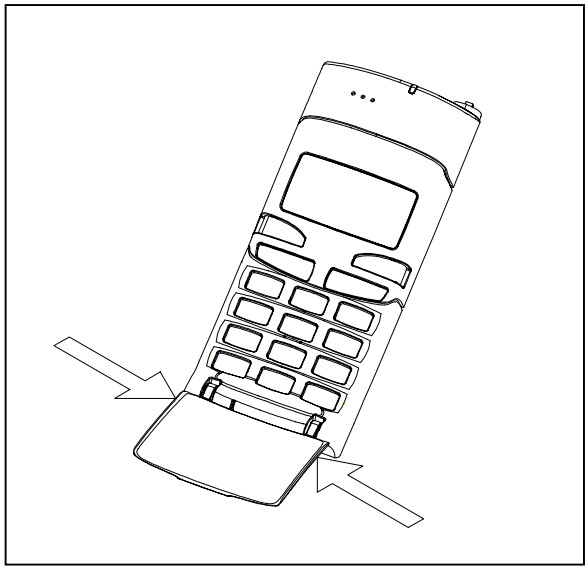


Figure 10-5

10.6 Changing the Keymat

10.6.1 Remove the volume button as described in 10.2 above.

10.6.2 Remove the back moulding as described in 10.3 above.

10.6.3 Remove the keymat from the front case/window assembly.

10.6.4 Fit new keymat as shown in Figure 10-6 below and reassemble the phone in reverse order.

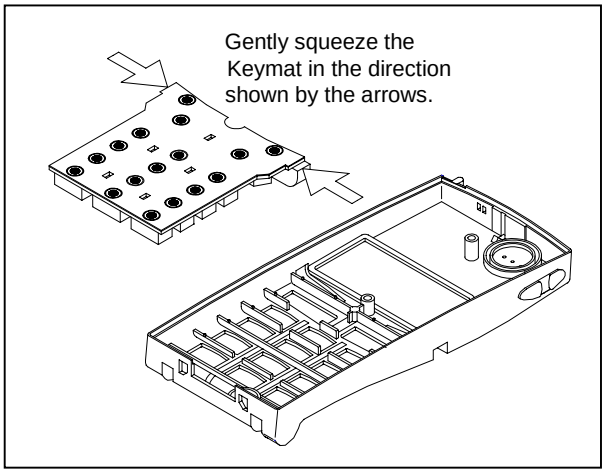



Figure 10-6

10.7 Changing the Microphone

10.7.1 Remove the volume button as described in 10.2 above.

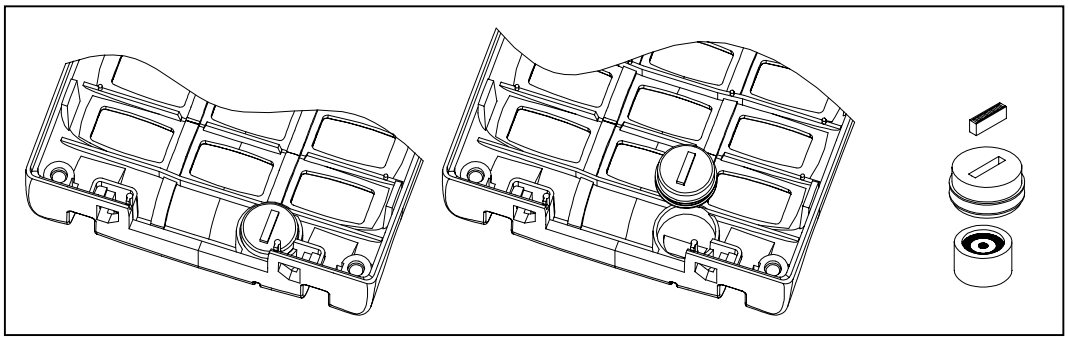


Figure 10-7

10.7.2 Remove the back moulding as described in 10.3 above.

10.7.3 Remove the microphone assembly out of the recess in the front case using tweezers as shown in Figure 10-7 above.

10.7.4 Extract the microphone from inside the microphone gasket and retain the zebra strip and microphone gasket.

10.7.5 Fit new microphone into the microphone gasket. Ensure that the end of the microphone having the gold coaxial contacts is inserted first into the microphone gasket (see Figure 10-7 above) and that the microphone is fully inserted into the microphone gasket.

10.7.6 Insert zebra strip into the slot at the top of the microphone boot. Ensure that the conductive stripes on the zebra strip are visible. See Figure 10-7 above.

10.7.7 Fit the microphone assembly in the recess in the front case ensuring that the zebra strip is oriented as shown in Figure 10-7 above.

***Caution – Take care not to damage the front face of the Microphone.***

10.8 Changing the Speaker

10.8.1 Remove the volume button as described in 10.2 above.

10.8.2 Remove the back moulding as described in 10.3 above.

10.8.3 Remove the PCB assembly as described in 10.4 above.

10.8.4 Lift out the zebra strip and retain.

10.8.5 Prise the Speaker from the front case/window assembly using a small jewellers screwdriver or similar.

10.8.6 Re-assemble as shown in Figure 10-8 overleaf.

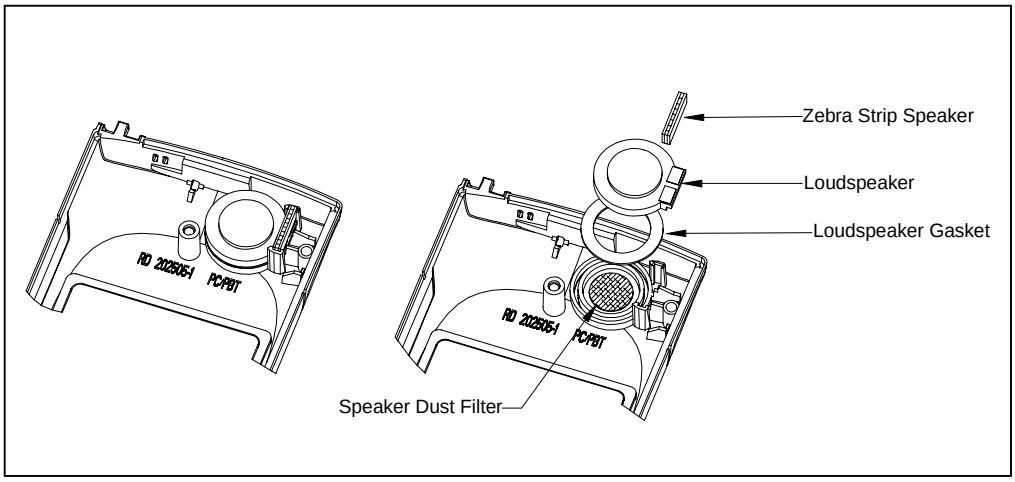



Figure 10.8

10.9 Changing the LCD Panel

10.9.1 Remove the volume button as described in 10.2 above.

10.9.2 Remove the back moulding as described in 10.3 above.

10.9.3 Remove the PCB assembly as described in 10.4 above.

10.9.4 Release 2 catches as shown in Figure 10-9 below and remove the LCD panel from the display holder.

10.9.5 Lift the ZIF connector-locking bar and extract the LCD panel flexi-tail.

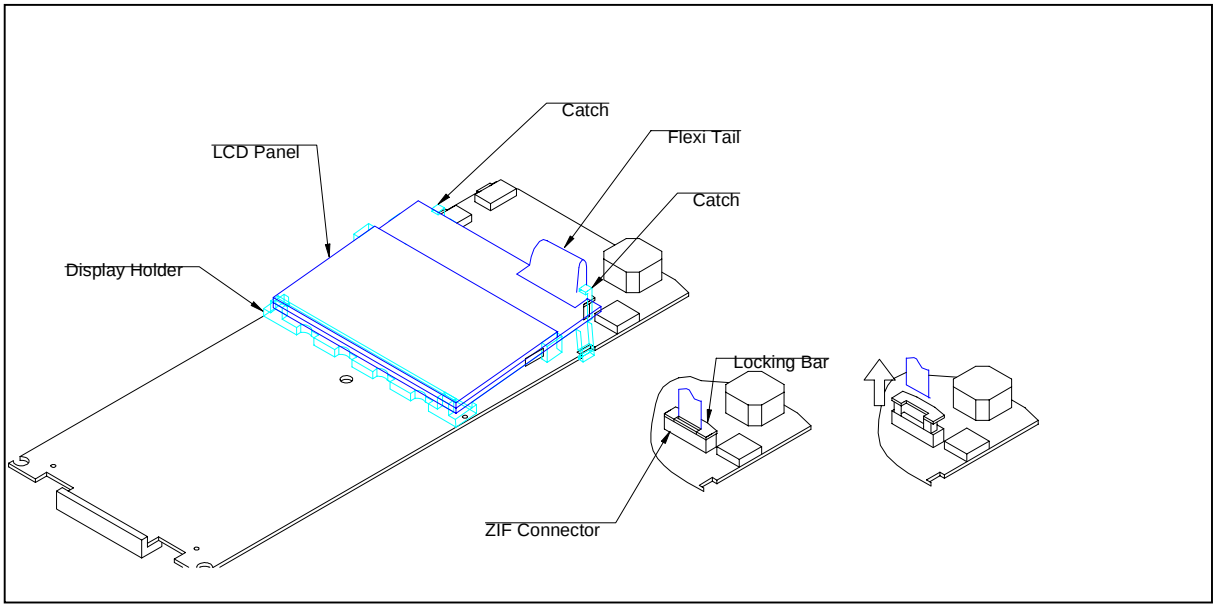



Figure 10-9

10.9.6 Reassemble in reverse order taking care to ensure that the LCD panel flexi tail is fully inserted into the ZIF connector before the locking bar is pushed down.

10.10 Reassembling the phone

10.10.1 Fit the transceiver part of the PCB assembly into the back moulding, as shown in Figure 10-10 below taking care to ensure that the antenna contact is not damaged.

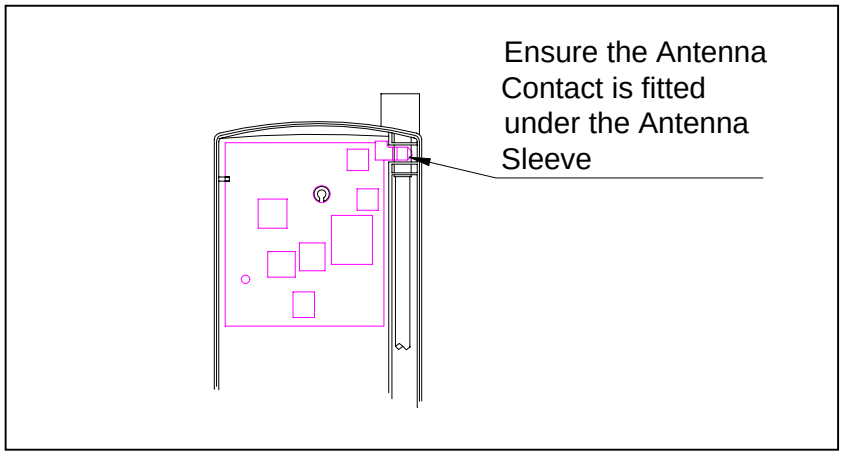



Figure 10-10

10.10.2 Fit the screw, as shown in Figure 10-11 below, and tighten to a torque setting of 0.32 Nm using a torque driver fitted with a T6 X 60 adapter.

10.10.3 Fit the distance sleeve ensuring that it is orientated correctly as shown in Figure 10-11 below.

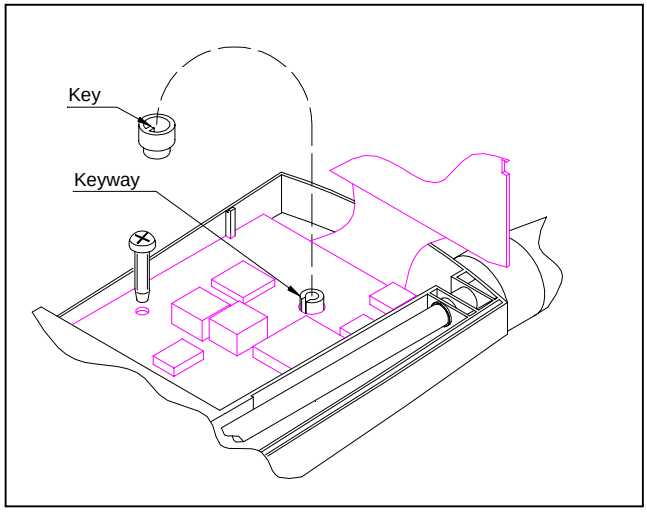



Figure 10-11

10.10.4 Fold the main part of the PCB assembly flat onto the back moulding ensuring the fixing holes in the PCB align with the appropriate holes in the back moulding. Ensure that locating spigots on the back moulding engage in the appropriate holes in the PCB assembly.

10.10.5 Offer the front case/window assembly to the back moulding and PCB engaging the tongue on the front case, adjacent to the antenna mounting, into the recess in the back moulding. Lower the front case onto the back moulding.

Drawing showing how to assemble the front and rear case goes here – not yet drawn.

10.10.6 Insert 3 screws 12mm long and 1 screw 5mm long as shown in Figure 10-12. Tighten to a torque of 0.32 Nm using a torque driver fitted with a T6 X 60 adapter.

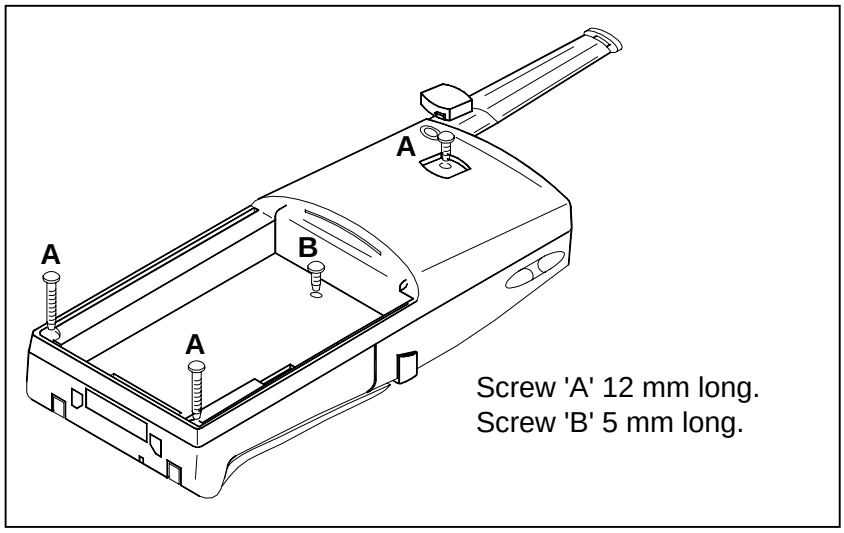



Figure 10-12

10.10.7 Refit the clip hole moulding.

10.10.8 Refit the battery pack.

10.10.9 Perform basic functional testing of the phone.

# 11 Fault Diagnosis

**NOTES**

# 12 Mechanical Assembly Diagrams and Parts Lists

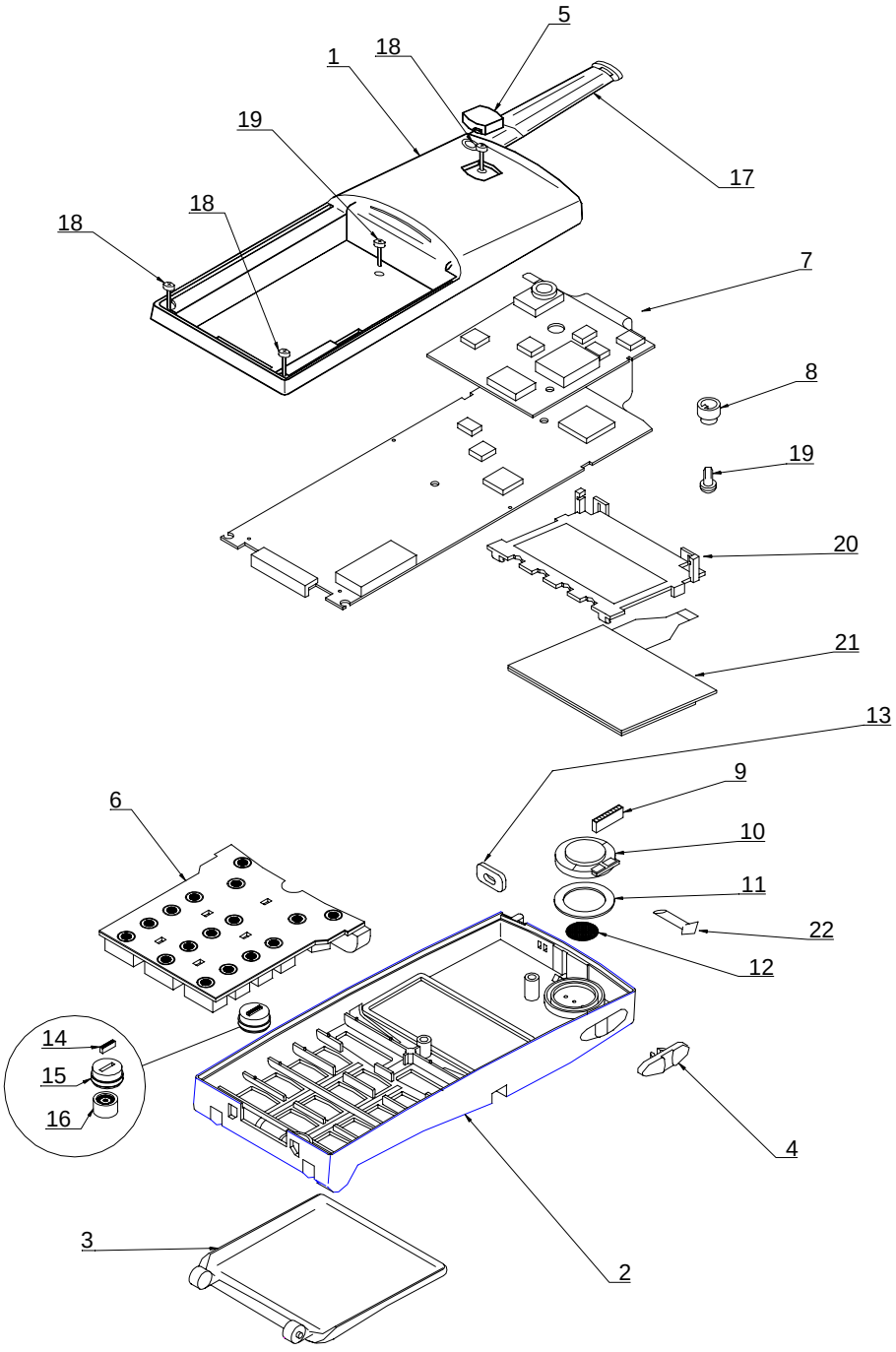



Figure 12-1

| Item | Description | Qty | Part Number |
|---|---|---|---|
| 1 | Back Moulding Metalised | 1 | 31005-001 |
| 2 | Front Case/Window Assy | 1 | See Table 15-2 |
| 3 | Cover Mould | 1 | See Table 15-2 |
| 4 | Volume Button | 1 | 32001-001 |
| 5 | Clip Hole Mould | 1 | 32002-001 |
| 6 | Terminal A1 Keyboard Hard | 1 | See Table 15-2 |
| 7 | PCB Assembly | 1 | See Table 15-3 |
| 8 | Distance Sleeve | 1 | 32003-001 |
| 9 | Zebra Strip Speaker | 1 | 73901-001 |
| 10 | Loudspeaker | 1 | 68002-001 |
| 11 | Loudspeaker Gasket | 1 | 35303-001 |
| 12 | Speaker Dust Filter | 1 | 35501-001 |
| 13 | Gasket Buzzer | 1 | 35304-001 |
| 14 | Zebra Strip – Microphone 2.7 | 1 | 73902-001 |
| 15 | Microphone Gasket 2.7 mm | 1 | 35301-001 |
| 16 | Microphone | 1 | 68003-001 |
| 17 | Terminal A1 Antenna | 1 | See Table 15-3 |
| 18 | Screw Torx Hd 2.2mm X | 3 | 82002-120 |
| 19 | Screw Torx Hd 2.2mm X 5mm | 2 | 82002-050 |
| | | | |

Table 12-1

| Item | Description | Colour/Branding | Part Number |
|---|---|---|---|
| 2a | Front Case/Window Assy | Black RDL A66 | 08501-001 |
| 2b | | Green RDL A66 | 08501-002 |
| 2c | | Blue RDL A66 | 08501-003 |
| 2d | | Grey RDL A66 | 08501-004 |
| | | | |
| 3a | Cover Moulding | Black RDL | 31003-001 |
| 3b | | GreenRDL | 31003-002 |
| 3c | | Blue RDL | 31003-003 |
| 3d | | Grey RDL | 31003-004 |
| | | | |
| 6a | Keymat | Latin | 35201-001 |
| 6b | | Cyrillic | 35201-002 |
| | | | |

Table 12-2

| Item | Description | Band | Part Number |
|---|---|---|---|
| 7a | PCB Assembly | Band 1:3 | 21001.001 |
| 7b | PCB Assembly | Band 5 | 21001-005 |
| | | | |
| 17a | Terminal A1 Antenna | Band 1:3 | 7901-001 |
| 17b | Terminal A1 Antenna | Band 5 | 7901-001 |

Table 12-3

# 13 Circuit Diagrams, PCB Assembly Diagrams and Parts Lists

| CCT ref | Tellit P/n. | Description | Value | Tolerance | Rating | Type | Side | X Position | Y Position |
|---|---|---|---|---|---|---|---|---|---|
| BU1 | 68001-001 | SOUNDER | | | | | Side 1 | 32.9 | 101.0 |
| C1 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | | Side 1 | 12.0 | 142.9 |
| C101 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 13.3 | 9.3 |
| C102 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 20.2 | 9.9 |
| C103 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 17.6 | 9.9 |
| C104 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 18.9 | 9.9 |
| C105 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 16.4 | 9.9 |
| C106 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 21.5 | 9.9 |
| C107 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 22.7 | 9.9 |
| C108 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 24.0 | 9.9 |
| C109 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | | Side 2 | 25.3 | 9.9 |
| C110 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | | Side 2 | 27.0 | 9.9 |
| C111 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | | Side 1 | 26.3 | 95.6 |
| C112 | 53311-104 | CAP CER | 100nF | +/-10% | 50V | | Side 1 | 35.0 | 90.2 |
| C113 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 8.3 | 27.4 |
| C114 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 7.1 | 27.4 |
| C115 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 2.6 | 32.8 |
| C116 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | | Side 2 | 4.7 | 26.8 |
| C201 | 54303-226 | CAP TANT | 22uF | +/-20% | 6V | | Side 2 | 40.8 | 7.5 |
| C202 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | | Side 2 | 2.9 | 62.0 |
| C203 | 54103-225 | CAP TANT | 2.2uF | +/-20% | 10V | | Side 2 | 31.2 | 63.5 |
| C204 | 54203-106 | CAP TANT | 10uF | +/-20% | 6V | | Side 2 | 21.7 | 63.6 |
| C205 | 54203-106 | CAP TANT | 10uF | +/-20% | 6V | | Side 2 | 18.4 | 63.6 |
| C206 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | | Side 2 | 3.9 | 67.8 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| C207 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 2 | 26.6 | 68.1 |
| C208 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 11.0 | 71.3 |
| C209 | 54103-225 | CAP TANT | 2.2uF | +/-20% | 10V | Side 2 | 36.3 | 73.7 |
| C211 | 54103-225 | CAP TANT | 2.2uF | +/-20% | 10V | Side 2 | 28.4 | 74.7 |
| C212 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 37.2 | 65.9 |
| C213 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 30.2 | 65.8 |
| C214 | 54103-225 | CAP TANT | 2.2uF | +/-20% | 10V | Side 2 | 35.4 | 63.5 |
| C301 | 53304-220 | CAP CER | 22pF | | | Side 1 | 4.8 | 80.2 |
| C302 | 53304-220 | CAP CER | 22pF | | | Side 1 | 8.6 | 80.3 |
| C303 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 2 | 11.3 | 83.1 |
| C304 | 53306-331 | CAP CER | 330pF | +/-5% | 50V | Side 1 | 32.3 | 76.8 |
| C305 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 1 | 29.8 | 87.9 |
| C306 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 1 | 31.8 | 88.0 |
| C307 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 2 | 26.2 | 79.4 |
| C308 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 32.5 | 83.4 |
| C309 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 35.8 | 82.8 |
| C310 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 1 | 33.0 | 87.8 |
| C311 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 31.7 | 84.4 |
| C312 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 31.9 | 82.7 |
| C313 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 36.4 | 97.9 |
| C314 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 1 | 32.8 | 75.3 |
| C315 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 2.5 | 64.3 |
| C316 | 53311-224 | CAP CER | 220nF | +/-10% | 16V | Side 1 | 4.1 | 70.1 |
| C317 | 53306-471 | CAP CER | 470pF | +/-5% | 50V | Side 1 | 11.8 | 73.1 |
| C318 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 2 | 14.6 | 9.5 |
| C319 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 34.3 | 62.1 |
| C320 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 2 | 22.7 | 66.7 |
| C401 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 3.5 | 86.0 |
| C402 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | Side 2 | 3.6 | 84.5 |
| C403 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 4.2 | 83.4 |
| C404 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 11.4 | 75.1 |
| C405 | 53304-220 | CAP CER | 22pF | | | Side 2 | 10.7 | 85.2 |

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|---|---|---|---|---|---|---|---|---|
| C406 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 6.2 | 85.9 |
| C407 | 53311-473 | CAP CER | 47nF | +/-10% | 16V | Side 2 | 18.6 | 102.2 |
| C408 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 8.1 | 72.7 |
| C409 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 5.0 | 72.6 |
| C410 | 53311-473 | CAP CER | 47nF | +/-10% | 16V | Side 2 | 13.2 | 84.2 |
| C411 | | NOTFITTED | | | | Side 2 | 19.9 | 85.4 |
| C414 | 53311-473 | CAP CER | 47nF | +/-10% | 16V | Side 2 | 4.3 | 88.5 |
| C415 | 53306-221 | CAP CER | 220pF | +/-5% | 50V | Side 2 | 20.8 | 95.9 |
| C420 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 1 | 10.1 | 95.8 |
| C421 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 22.1 | 97.8 |
| C422 | 53311-473 | CAP CER | 47nF | +/-10% | 16V | Side 1 | 15.9 | 98.8 |
| C423 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 12.6 | 95.8 |
| C424 | 53311-473 | CAP CER | 47nF | +/-10% | 16V | Side 2 | 7.2 | 102.4 |
| C425 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 1 | 8.4 | 92.5 |
| C426 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 2.1 | 92.1 |
| C427 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 6.3 | 87.5 |
| C428 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 2.1 | 88.9 |
| C429 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 3.8 | 96.4 |
| C430 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 2.2 | 94.2 |
| C431 | | NOTFITTED | | | | Side 1 | 11.7 | 93.2 |
| C440 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 2 | 31.6 | 97.7 |
| C441 | | NOTFITTED | | | | Side 2 | 4.8 | 100.7 |
| C442 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 2.4 | 102.1 |
| C443 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 11.1 | 104.2 |
| C444 | 53306-101 | CAP CER | 100pF | +/-5% | 50V | Side 2 | 10.3 | 102.1 |
| C445 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 6.8 | 72.1 |
| C446 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 15.8 | 102.1 |
| C447 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 15.8 | 100.8 |
| C501 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 17.4 | 127.9 |
| C502 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 1 | 16.3 | 120.2 |
| C503 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 11.0 | 123.8 |
| C504 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 1 | 12.9 | 120.3 |

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|---|---|---|---|---|---|---|---|---|
| C505 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 1 | 1.5 | 126.0 |
| C506 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 1.3 | 119.5 |
| C507 | 53306-471 | CAP CER | 470pF | +/-5% | 50V | Side 1 | 2.0 | 122.5 |
| C508 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 9.8 | 116.5 |
| C509 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 1 | 10.4 | 118.2 |
| C510 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 9.8 | 119.8 |
| C511 | 61302-100 | INDUCTOR | 10nH | 2% | | Side 1 | 14.2 | 116.4 |
| C512 | 53301-082 | CAP CER | 8.2pF | +/-0.25pF | 50V | Side 1 | 16.8 | 116.2 |
| C513 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 20.9 | 120.1 |
| C514 | 54203-106 | CAP CER | 10uF | +/-20% | 6V | Side 1 | 23.9 | 120.8 |
| C515 | 53301-047 | CAP CER | 4.7pF | | | Side 1 | 27.4 | 116.9 |
| C516 | 53301-056 | CAP CER | 5.6pF | | | Side 1 | 25.5 | 117.4 |
| C517 | 53301-047 | CAP CER | 4.7pF | | | Side 2 | 35.0 | 120.5 |
| C518 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 2 | 29.7 | 122.0 |
| C519 | 53311-473 | CAP CER | 47nF | +/-10% | 16V | Side 2 | 7.8 | 114.7 |
| C521 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 2 | 27.5 | 117.1 |
| C601 | 54104-335 | CAP CER | 3.3uF | +/-20% | 6V | Side 1 | 22.0 | 143.2 |
| C602 | 53306-471 | CAP CER | 470pF | +/-5% | 50V | Side 1 | 15.0 | 136.7 |
| C603 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 2 | 21.4 | 131.5 |
| C604 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 18.7 | 128.1 |
| C605 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 2 | 36.0 | 139.7 |
| C606 | 53304-150 | CAP CER | 15pF | | | Side 1 | 22.5 | 132.2 |
| C607 | 53311-473 | CAP CER | 47nF | +/-10% | 16V | Side 1 | 15.1 | 140.9 |
| C608 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 1 | 15.2 | 143.8 |
| C609 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 1 | 1.6 | 134.7 |
| C610 | 53309-332 | CAP CER | 3.3nF | +/-10% | 50V | Side 1 | 1.6 | 140.1 |
| C611 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 16.8 | 131.9 |
| C612 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | Side 1 | 4.7 | 150.2 |
| C613 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 1 | 4.6 | 151.8 |
| C614 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 1 | 20.3 | 148.7 |
| C615 | 53306-471 | CAP CER | 470pF | +/-5% | 50V | Side 1 | 4.7 | 148.4 |
| C616 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 21.8 | 153.1 |

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|---|---|---|---|---|---|---|---|---|
| C617 | 53311-224 | CAP CER | 220nF | +/-10% | 16V | Side 1 | 15.1 | 142.3 |
| C618 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 2 | 36.0 | 137.2 |
| C619 | 53306-471 | CAP CER | 470pF | +/-5% | 50V | Side 1 | 15.0 | 138.9 |
| C620 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 20.8 | 116.4 |
| C621 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 2 | 18.8 | 119.7 |
| C622 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 1 | 29.6 | 148.9 |
| C623 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 26.2 | 121.9 |
| C624 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 1 | 30.6 | 152.1 |
| C701 | 53301-082 | CAP CER | 8.2pF | +/-0.25pF | 50V | Side 1 | 33.1 | 131.7 |
| C702 | 53309-332 | CAP CER | 3.3nF | +/-10% | 50V | Side 1 | 30.3 | 131.3 |
| C703 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 29.2 | 129.5 |
| C704 | 53309-332 | CAP CER | 3.3nF | +/-10% | 50V | Side 1 | 29.0 | 140.2 |
| C705 | 53309-332 | CAP CER | 3.3nF | +/-10% | 50V | Side 1 | 34.4 | 131.5 |
| C706 | 53301-027 | CAP CER | 2.7pF | | | Side 1 | 31.9 | 137.1 |
| C707 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 28.8 | 136.1 |
| C708 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 1 | 28.0 | 143.7 |
| C718 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 2 | 17.2 | 130.6 |
| C719 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 17.5 | 128.6 |
| C720 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 2 | 5.3 | 122.5 |
| C721 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 2 | 14.6 | 136.0 |
| C722 | 54104-335 | CAP TANT | 3.3uF | +/-20% | 6V | Side 2 | 20.5 | 134.7 |
| C723 | 53212-105 | CAP CER | 1uF | +/-10% | 10V | Side 2 | 13.6 | 122.2 |
| C724 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 2 | 12.0 | 137.0 |
| C725 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 12.4 | 135.2 |
| C726 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 2 | 13.2 | 137.0 |
| C727 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | Side 2 | 8.1 | 121.2 |
| C728 | 53301-056 | CAP CER | 5.6pF | | | Side 1 | 33.0 | 153.8 |
| C729 | 53301-022 | CAP CER | 2.2pF | | | Side 1 | 28.3 | 155.5 |
| C730 | 53311-104 | CAP CER | 100nF | +/-10% | 16V | Side 2 | 25.5 | 146.9 |
| C731 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | Side 2 | 27.6 | 146.5 |
| C732 | 53306-680 | CAP CER | 68pF | | | Side 2 | 25.6 | 149.6 |
| C733 | 53304-330 | CAP CER | 33pF | | | Side 2 | 27.5 | 150.3 |

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|---|---|---|---|---|---|---|---|---|---|
| C734 | 53304-120 | CAP CER | 12pF | | | | Side 2 | 26.2 | 151.6 |
| C735 | 53304-220 | CAP CER | 22pF | | | | Side 2 | 24.4 | 148.2 |
| C736 | 53301-082 | CAP CER | 8.2pF | | | | Side 2 | 22.4 | 151.8 |
| C737 | 53304-220 | CAP CER | 22pF | | | | Side 2 | 12.3 | 154.9 |
| C738 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 4.9 | 151.4 |
| C739 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 6.2 | 154.0 |
| C740 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 1.7 | 147.9 |
| C741 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 12.9 | 148.2 |
| C742 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 3.4 | 136.3 |
| C743 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 4.5 | 125.1 |
| C744 | 53306-221 | CAP CER | 220pF | +/-5% | 50V | | Side 2 | 3.4 | 135.0 |
| C745 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 1.5 | 126.1 |
| C747 | 53301-056 | CAP CER | 5.6pF | | | | Side 2 | 3.8 | 148.4 |
| C748 | 53301-100 | CAP CER | 10pF | | | | Side 2 | 8.9 | 151.1 |
| C749 | 53309-102 | CAP CER | 1nF | +/-10% | 50V | | Side 2 | 17.2 | 126.7 |
| C750 | 53306-151 | CAP CER | 150pF | +/-5% | 50V | | Side 1 | 30.1 | 154.5 |
| C751 | | NOTFITTED | | | | | Side 2 | 33.4 | 154.4 |
| C752 | 53301-010 | CAP CER | 1pF | | | | Side 2 | 32.2 | 154.4 |
| C753 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 5.5 | 127.6 |
| C754 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 4.5 | 130.6 |
| C755 | 53309-103 | CAP CER | 10nF | +/-10% | 50V | | Side 2 | 31.0 | 149.2 |
| | | | | | | | | | |
| D101 | 59002-001 | DIODE | | | | BAV99W | Side 1 | 33.5 | 5.5 |
| D102 | 59002-001 | DIODE | | | | BAV99W | Side 2 | 6.0 | 33.0 |
| D201 | 59003-001 | DIODE SCOTTKY | | | | STPS340U | Side 1 | 21.5 | 2.5 |
| D202 | 59002-001 | DIODE | | | | BAV99W | Side 2 | 4.6 | 70.5 |
| D204 | 59004-001 | DIODE SCOTTKY | | | | MBR520LT | Side 2 | 1.5 | 69.8 |
| D301 | 59002-001 | DIODE | | | | BAV99W | Side 1 | 36.3 | 67.2 |
| D302 | 59002-001 | DIODE | | | | BAV99W | Side 1 | 28.8 | 68.3 |
| D303 | 59701-001 | DIODE-LED RED/GREEN | | | | CL-155UR/G-D-T | Side 1 | 25.7 | 99.0 |
| D305 | 59703-001 | DIODE-LED | | | | CL-190YG-CD-T | Side 1 | 21.5 | 45.3 |
| D306 | 59703-001 | DIODE-LED | | | | CL-190YG-CD-T | Side 1 | 14.6 | 32.9 |

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|---|---|---|---|---|---|---|---|---|
| D307 | 59703-001 | DIODE-LED | | | CL-190YG-CD-T | Side 1 | 28.4 | 32.9 |
| D308 | 59703-001 | DIODE-LED | | | CL-190YG-CD-T | Side 1 | 14.6 | 16.0 |
| D309 | 59703-001 | DIODE-LED | | | CL-190YG-CD-T | Side 1 | 28.4 | 16.0 |
| D310 | 59702-001 | DIODE-LED YELL/GREEN | | | CL-220YG-C-TS | Side 1 | 8.7 | 57.0 |
| D311 | 59702-001 | DIODE-LED YELL/GREEN | | | CL-220YG-C-TS | Side 1 | 17.2 | 57.0 |
| D312 | 59702-001 | DIODE-LED YELL/GREEN | | | CL-220YG-C-TS | Side 1 | 25.7 | 57.0 |
| D313 | 59702-001 | DIODE-LED YELL/GREEN | | | CL-220YG-C-TS | Side 1 | 34.2 | 57.0 |
| D314 | 59002-001 | DIODE | | | BAV99W | Side 2 | 27.2 | 62.8 |
| D700 | 59002-001 | DIODE | | | BAV99W | Side 1 | 33.3 | 128.7 |
| | | | | | | | | |
| J101 | 73101-001 | BATTERY CONNECTOR | | | | Side 2 | 4.4 | 16.1 |
| J102 | 73301-001 | CONNECTOR 52 8 POL | | | | Side 1 | 32.1 | 93.3 |
| J104 | 73102-001 | CONNECTOR 85 | | | | Side 2 | 21.5 | 2.0 |
| | | | | | | | | |
| L501 | 61701-001 | FERRITE-BEAD | | | | Side 1 | 2.1 | 128.7 |
| L502 | 61202-470 | INDUCTOR | 47nH | | | Side 1 | 4.2 | 121.7 |
| L503 | 53204-150 | CAP CER | 15pF | | | Side 1 | 16.4 | 117.6 |
| L504 | 61202-270 | INDUCTOR | 27nH | | | Side 1 | 21.5 | 117.2 |
| L505 | 61701-001 | FERRITE-BEAD | | | | Side 1 | 24.3 | 118.6 |
| L506 | 61202-180 | INDUCTOR | 18nH | | | Side 2 | 34.7 | 122.7 |
| L507 | 61202-180 | INDUCTOR | 18nH | | | Side 2 | 32.1 | 121.3 |
| L508 | 61202-100 | INDUCTOR | 10nH | 2% | | Side 1 | 25.1 | 116.0 |
| L601 | 61701-001 | FERRITE-BEAD | | | | Side 1 | 21.3 | 130.2 |
| L602 | 61701-001 | FERRITE-BEAD | | | | Side 1 | 1.5 | 131.3 |
| L603 | 61701-001 | FERRITE-BEAD | | | | Side 1 | 19.6 | 150.6 |
| L604 | 61202-270 | INDUCTOR | 27nH | | | Side 1 | 11.8 | 128.3 |
| L605 | 61701-001 | FERRITE-BEAD | | | | Side 1 | 16.9 | 138.6 |
| L701 | 61301-018 | INDUCTOR | 1.8nH | | | Side 1 | 29.9 | 133.9 |
| L703 | 61202-180 | INDUCTOR | 18nH | | | Side 1 | 31.7 | 131.5 |
| L704 | 61202-330 | INDUCTOR | 33nH | | | Side 1 | 29.6 | 137.7 |
| L707 | 61202-330 | INDUCTOR | 33nH | | | Side 2 | 33.6 | 152.2 |
| L709 | 61701-001 | FERRITE-BEAD | | | | Side 2 | 16.2 | 134.2 |

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|---|---|---|---|---|---|---|---|
| L710 | 61202-470 | INDUCTOR | 47nH | | Side 1 | 33.7 | 151.7 |
| L711 | 61110-471 | INDUCTOR | 0.47nH | | Side 2 | 28.2 | 148.5 |
| L712 | 61110-471 | INDUCTOR | 0.47nH | | Side 2 | 22.6 | 148.5 |
| L713 | 61110-561 | INDUCTOR | 0.56nH | | Side 2 | 13.8 | 152.1 |
| L714 | 61202-470 | INDUCTOR | 47nH | | Side 2 | 3.4 | 133.6 |
| L715 | 61701-001 | FERRITE-BEAD | | | Side 2 | 4.2 | 154.1 |
| L716 | 61701-001 | FERRITE-BEAD | | | Side 2 | 1.4 | 134.4 |
| L719 | 61701-001 | FERRITE-BEAD | | | Side 1 | 27.5 | 141.8 |
| L720 | 61110-152 | INDUCTOR | 1.5uH | | Side 2 | 2.0 | 151.3 |
| L721 | 61110-821 | INDUCTOR | 0.82nH | | Side 2 | 11.2 | 151.4 |
| L722 | 61701-001 | FERRITE-BEAD | | | Side 2 | 26.0 | 144.3 |
| L723 | 61202-470 | INDUCTOR | 47nH | | Side 1 | 32.3 | 155.3 |
| | | | | | | | |
| Q101 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 2 | 40.1 | 17.1 |
| Q102 | 69002-001 | TRANSISTOR PNP | | BC857BW | Side 2 | 41.4 | 13.8 |
| Q103 | 69002-001 | TRANSISTOR PNP | | BC857BW | Side 2 | 40.4 | 19.9 |
| Q201 | 69008-001 | TRANSISTOR P-MOS | | SI3443DV | Side 2 | 2.4 | 29.1 |
| Q202 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 2 | 14.1 | 75.8 |
| Q203 | 69002-001 | TRANSISTOR PNP | | BC857BW | Side 1 | 21.6 | 64.3 |
| Q204 | 69002-001 | TRANSISTOR PNP | | BC857BW | Side 1 | 18.2 | 64.2 |
| Q301 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 1 | 3.4 | 66.7 |
| Q302 | 69007-001 | TRANSISTOR N-MOS | | TN0200T | Side 1 | 2.9 | 75.1 |
| Q304 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 1 | 39.2 | 86.2 |
| Q305 | 69006-001 | TRANSISTOR P-MOS | | TP0101T | Side 1 | 38.8 | 71.6 |
| Q306 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 1 | 35.4 | 70.9 |
| Q307 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 1 | 33.2 | 65.8 |
| Q308 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 1 | 25.5 | 67.4 |
| Q309 | 69001-001 | TRANSISTOR NPN | | BC848CW | Side 2 | 35.9 | 85.6 |
| Q501 | 69009-001 | TRANSISTOR UHF | | BFG10W/X | Side 1 | 19.4 | 117.0 |
| Q601 | 69006-001 | TRANSISTOR P-MOS | | TP0101T | Side 1 | 25.7 | 153.7 |
| Q701 | 69004-001 | TRANSISTOR UHF | | BFP420 | Side 1 | 32.5 | 134.4 |
| Q702 | 69005-001 | GaAs Dual Gate FET | | CF739 | Side 2 | 30.2 | 151.9 |

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|---|---|---|---|---|---|---|---|---|---|
| Q703 | 69003-001 | TRANSISTOR RF NPN | | | | BFR92AW | Side 2 | 6.6 | 149.5 |
| Q704 | 69003-001 | TRANSISTOR RF NPN | | | | BFR92AW | Side 2 | 9.9 | 147.7 |
| Q705 | 69003-001 | TRANSISTOR RF NPN | | | | BFR92AW | Side 2 | 3.1 | 128.5 |
| | | | | | | | | | |
| R101 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 15.7 | 7.0 |
| R102 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 17.0 | 7.0 |
| R103 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 18.3 | 7.0 |
| R104 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 19.5 | 7.0 |
| R105 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 20.8 | 7.0 |
| R106 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 22.1 | 7.0 |
| R107 | 64301-100 | RES CHIP | 10R | +/-1% | 0.1W | | Side 2 | 23.4 | 7.0 |
| R108 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 24.6 | 7.0 |
| R109 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | | Side 2 | 27.0 | 7.0 |
| R110 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | | Side 2 | 7.9 | 34.0 |
| R111 | 64301-474 | RES CHIP | 470k | +/-1% | 0.1W | | Side 2 | 30.0 | 93.6 |
| R112 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | | Side 2 | 29.6 | 7.0 |
| R113 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | | Side 2 | 16.3 | 72.6 |
| R114 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | | Side 1 | 37.7 | 62.1 |
| R115 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | | Side 2 | 42.2 | 17.1 |
| R116 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | | Side 2 | 41.4 | 11.6 |
| R117 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | | Side 2 | 39.5 | 12.1 |
| R118 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | | Side 2 | 2.3 | 34.7 |
| R119 | 64301-223 | RES CHIP | 22k | +/-1% | 0.1W | | Side 2 | 8.0 | 31.6 |
| R120 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | | Side 1 | 40.1 | 63.1 |
| R121 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | | Side 2 | 39.5 | 14.4 |
| R122 | 64301-000 | RES CHIP | 0R | | | | Side 2 | 39.9 | 30.9 |
| R201 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | | Side 2 | 4.9 | 29.7 |
| R202 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | | Side 2 | 6.2 | 29.8 |
| R203 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | | Side 2 | 2.7 | 31.6 |
| R204 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | | Side 2 | 14.5 | 73.8 |
| R205 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | | Side 2 | 7.5 | 71.2 |
| R207 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | | Side 2 | 16.4 | 75.9 |

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|---|---|---|---|---|---|---|---|---|
| R208 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 2 | 26.7 | 76.0 |
| R209 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 24.7 | 76.3 |
| R210 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 23.4 | 76.2 |
| R211 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 27.4 | 70.6 |
| R212 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 1 | 21.5 | 99.6 |
| R213 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 1 | 20.3 | 99.6 |
| R215 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 2 | 15.3 | 64.9 |
| R216 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 1 | 20.6 | 62.1 |
| R217 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 1 | 23.0 | 62.2 |
| R218 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 1 | 17.1 | 66.4 |
| R219 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 1 | 18.3 | 67.8 |
| R220 | 64301-473 | RES CHIP | 47k | +/-1% | 0.1W | Side 1 | 20.0 | 65.7 |
| R221 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 23.7 | 64.1 |
| R222 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 2 | 31.1 | 80.5 |
| R223 | 64301-000 | RES CHIP | 0R | | | Side 2 | 28.8 | 79.2 |
| R224 | | NOTFITTED | | | | Side 2 | 36.5 | 76.6 |
| R238 | 64301-393 | RES CHIP | 39k | +/-1% | 0.1W | Side 2 | 35.3 | 70.0 |
| R239 | 67101-001 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 36.6 | 70.0 |
| R240 | 64301-100 | RES CHIP | 10R | +/-1% | 0.1W | Side 2 | 27.8 | 68.7 |
| R241 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 2 | 30.2 | 68.4 |
| R242 | 64301-683 | RES CHIP | 68k | +/-1% | 0.1W | Side 2 | 28.9 | 68.7 |
| R243 | 64301-114 | RES CHIP | 110k | +/-1% | 0.1W | Side 2 | 34.1 | 70.0 |
| R244 | 64301-223 | RES CHIP | 22k | +/-1% | 0.1W | Side 1 | 10.5 | 65.7 |
| R245 | 64301-223 | RES CHIP | 22k | +/-1% | 0.1W | Side 1 | 10.5 | 64.5 |
| R246 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 1.6 | 65.2 |
| R247 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 2.9 | 65.2 |
| R248 | 64301-000 | RES CHIP | 0R | | | Side 1 | 8.9 | 98.8 |
| R249 | 64301-000 | RES CHIP | 0R | | | Side 2 | 32.8 | 70.0 |
| R300 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 29.7 | 89.1 |
| R301 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 1 | 13.9 | 97.5 |
| R302 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 2 | 29.8 | 101.6 |
| R303 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 2 | 34.8 | 101.1 |

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|---|---|---|---|---|---|---|---|---|
| R304 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 2 | 34.2 | 97.2 |
| R305 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 1 | 12.9 | 93.2 |
| R306 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 2 | 32.5 | 101.2 |
| R307 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 1 | 38.7 | 66.5 |
| R308 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 1 | 37.3 | 87.4 |
| R309 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | Side 1 | 36.5 | 85.1 |
| R310 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | Side 2 | 26.3 | 84.0 |
| R311 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 1 | 32.7 | 71.6 |
| R312 | 64301-000 | RES CHIP | 0R | | | Side 1 | 35.0 | 87.6 |
| R313 | 64301-474 | RES CHIP | 470k | +/-1% | 0.1W | Side 1 | 32.2 | 80.1 |
| R314 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 38.9 | 69.6 |
| R315 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | Side 2 | 36.2 | 93.2 |
| R316 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 1 | 33.1 | 69.7 |
| R317 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 31.7 | 79.0 |
| R318 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | Side 1 | 9.7 | 101.1 |
| R319 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 13.0 | 73.3 |
| R320 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 16.3 | 71.6 |
| R321 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 15.6 | 68.8 |
| R322 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 18.9 | 70.9 |
| R323 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 19.5 | 68.4 |
| R324 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 20.4 | 70.9 |
| R325 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 8.0 | 72.3 |
| R326 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 9.2 | 73.2 |
| R327 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 10.7 | 70.8 |
| R328 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 5.2 | 77.0 |
| R329 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 1 | 17.1 | 99.4 |
| R330 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 6.2 | 67.1 |
| R331 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 1.8 | 70.1 |
| R332 | 64301-472 | RES CHIP | 4k7 | +/-1% | 0.1W | Side 1 | 5.1 | 63.9 |
| R333 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 1.8 | 72.4 |
| R334 | 64301-391 | RES CHIP | 390k | +/-1% | 0.1W | Side 2 | 26.4 | 97.5 |
| R335 | 64301-391 | RES CHIP | 390k | +/-1% | 0.1W | Side 2 | 28.7 | 99.7 |

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|---|---|---|---|---|---|---|---|---|
| R336 | 64301-152 | RES CHIP | 1k5 | +/-1% | 0.1W | Side 1 | 25.6 | 70.3 |
| R337 | 64301-152 | RES CHIP | 1k5 | +/-1% | 0.1W | Side 1 | 23.0 | 70.9 |
| R338 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 21.8 | 70.9 |
| R339 | 64301-180 | RES CHIP | 18R | +/-1% | 0.1W | Side 1 | 31.3 | 66.2 |
| R340 | 64301-180 | RES CHIP | 18R | +/-1% | 0.1W | Side 1 | 23.6 | 68.2 |
| R341 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 29.6 | 71.6 |
| R342 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 30.7 | 70.1 |
| R343 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 38.1 | 83.1 |
| R344 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 31.8 | 74.2 |
| R345 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | Side 1 | 32.5 | 82.3 |
| R346 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 2 | 33.2 | 86.6 |
| R347 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 2 | 36.2 | 82.6 |
| R348 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 33.0 | 85.6 |
| R349 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 36.5 | 83.9 |
| R350 | 64301-333 | RES CHIP | 33k | +/-1% | 0.1W | Side 2 | 25.3 | 86.6 |
| R351 | 64301-100 | RES CHIP | 10R | +/-1% | 0.1W | Side 2 | 28.9 | 85.9 |
| R352 | 64301-100 | RES CHIP | 10R | +/-1% | 0.1W | Side 2 | 36.2 | 81.3 |
| R354 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 29.0 | 83.4 |
| R355 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 1 | 27.6 | 90.2 |
| R356 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | Side 2 | 20.8 | 81.5 |
| R357 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | Side 1 | 16.2 | 93.5 |
| R380 | 67101-001 | RES CHIP | 10k | +/-1% | | Side 1 | 32.6 | 84.5 |
| R381 | 67201-001 | RES-CHIP Voltage Suppressor 9Vwm | | | | Side 1 | 40.9 | 68.7 |
| R401 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | Side 2 | 2.5 | 87.5 |
| R402 | 64301-222 | RES CHIP | 2k2 | +/-1% | 0.1W | Side 2 | 1.5 | 85.4 |
| R403 | 64301-153 | RES CHIP | 15k | +/-1% | 0.1W | Side 2 | 1.7 | 83.4 |
| R404 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 2 | 9.4 | 84.8 |
| R405 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 8.2 | 84.1 |
| R406 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 7.0 | 84.1 |
| R407 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 2 | 12.6 | 102.7 |
| R408 | 64301-224 | RES CHIP | 220k | +/-1% | 0.1W | Side 2 | 12.6 | 101.6 |

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| R410 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 17.0 | 85.3 |
| R411 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 2 | 18.6 | 85.4 |
| R412 | 64301-100 | RES CHIP | 10R | +/-1% | 0.1W | Side 2 | 1.3 | 75.3 |
| R413 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 2 | 1.5 | 80.9 |
| R414 | 64301-104 | RES CHIP | 100k | +/-1% | 0.1W | Side 2 | 1.0 | 77.7 |
| R420 | 64301-105 | RES CHIP | 1M0 | +/-1% | 0.1W | Side 1 | 10.7 | 98.4 |
| R421 | 64301-473 | RES CHIP | 47k | +/-1% | 0.1W | Side 1 | 11.9 | 98.4 |
| R422 | 64301-473 | RES CHIP | 47k | +/-1% | 0.1W | Side 1 | 11.4 | 95.8 |
| R423 | 64301-332 | RES CHIP | 3k3 | +/-1% | 0.1W | Side 1 | 10.4 | 93.2 |
| R424 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 11.0 | 91.3 |
| R425 | 64301-563 | RES CHIP | 56k | +/-1% | 0.1W | Side 2 | 2.2 | 90.6 |
| R429 | 64301-100 | RES CHIP | 10R | +/-1% | 0.1W | Side 1 | 9.6 | 76.9 |
| R430 | 64301-103 | RES CHIP | 10R | +/-1% | 0.1W | Side 2 | 4.7 | 102.6 |
| R431 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 5.7 | 99.5 |
| R432 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 9.1 | 101.8 |
| R433 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 5.9 | 102.8 |
| R434 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 10.8 | 72.5 |
| R435 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 2 | 13.8 | 81.5 |
| R440 | | NOTFITTED | | | | Side 2 | 12.8 | 73.2 |
| R501 | 64301-821 | RES CHIP | 820R | +/-1% | 0.1W | Side 1 | 13.9 | 119.0 |
| R502 | 64301-152 | RES CHIP | 1k5 | +/-1% | 0.1W | Side 1 | 17.2 | 119.1 |
| R503 | 64301-221 | RES CHIP | 220R | +/-1% | 0.1W | Side 1 | 22.9 | 116.6 |
| R504 | | NOTFITTED | | | | Side 1 | 19.8 | 119.6 |
| R505 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 2 | 8.4 | 116.7 |
| R506 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 10.2 | 115.3 |
| R603 | 64301-154 | RES CHIP | 150k | +/-1% | 0.1W | Side 1 | 23.8 | 136.4 |
| R604 | 64301-822 | RES CHIP | 8k2 | +/-1% | 0.1W | Side 1 | 17.7 | 143.9 |
| R605 | 64301-333 | RES CHIP | 33k | +/-1% | 0.1W | Side 1 | 12.7 | 144.0 |
| R606 | 64301-221 | RES CHIP | 220R | +/-1% | 0.1W | Side 1 | 15.5 | 130.8 |
| R607 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 14.9 | 127.9 |
| R608 | 64301-180 | RES CHIP | 18R | +/-1% | 0.1W | Side 1 | 15.5 | 129.6 |
| R609 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 16.2 | 127.9 |

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|---|---|---|---|---|---|---|---|---|
| R610 | | NOTFITTED | | | | Side 1 | 17.3 | 141.8 |
| R611 | 64301-153 | RES CHIP | 15k | +/-1% | 0.1W | Side 1 | 2.5 | 150.9 |
| R612 | 64301-154 | RES CHIP | 150k | +/-1% | 0.1W | Side 1 | 6.6 | 149.3 |
| R613 | 64301-221 | RES CHIP | 220R | +/-1% | 0.1W | Side 1 | 19.3 | 153.1 |
| R614 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 19.1 | 152.0 |
| R615 | 64301-180 | RES CHIP | 18R | +/-1% | 0.1W | Side 1 | 19.3 | 155.0 |
| R616 | 64301-331 | RES CHIP | 330R | +/-1% | 0.1W | Side 1 | 22.5 | 155.0 |
| R617 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 1 | 25.0 | 151.5 |
| R618 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 1 | 27.3 | 151.4 |
| R619 | 64301-472 | RES CHIP | 4k7 | +/-1% | 0.1W | Side 1 | 23.9 | 140.3 |
| R620 | 64301-472 | RES CHIP | 4k7 | +/-1% | 0.1W | Side 1 | 22.1 | 141.5 |
| R701 | 64301-822 | RES CHIP | 8k2 | +/-1% | 0.1W | Side 1 | 35.7 | 131.4 |
| R702 | 64301-153 | RES CHIP | 15k | +/-1% | 0.1W | Side 1 | 30.5 | 128.2 |
| R703 | 64301-823 | RES CHIP | 82k | +/-1% | 0.1W | Side 1 | 28.4 | 131.2 |
| R704 | 64301-101 | RES CHIP | 100R | +/-1% | 0.1W | Side 1 | 27.0 | 136.7 |
| R705 | 64301-391 | RES CHIP | 390R | +/-1% | 0.1W | Side 1 | 29.6 | 139.1 |
| R706 | 64301-470 | RES CHIP | 47R | +/-1% | 0.1W | Side 1 | 30.6 | 135.7 |
| R707 | 64301-000 | RES CHIP | 0R | | | Side 1 | 32.1 | 148.8 |
| R708 | | NOTFITTED | | | | Side 1 | 34.0 | 148.3 |
| R709 | | NOTFITTED | | | | Side 1 | 33.9 | 149.5 |
| R710 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | Side 1 | 33.6 | 137.6 |
| R711 | 64301-120 | RES CHIP | 12R | +/-1% | 0.1W | Side 1 | 33.1 | 139.4 |
| R712 | 64301-471 | RES CHIP | 470R | +/-1% | 0.1W | Side 1 | 31.4 | 140.2 |
| R713 | 64301-683 | RES CHIP | 68k | +/-1% | 0.1W | Side 2 | 6.6 | 125.3 |
| R714 | 64301-564 | RES CHIP | 560k | +/-1% | 0.1W | Side 2 | 18.1 | 132.5 |
| R715 | 64301-154 | RES CHIP | 150k | +/-1% | 0.1W | Side 2 | 10.9 | 124.0 |
| R716 | 64301-154 | RES CHIP | 150k | +/-1% | 0.1W | Side 2 | 15.3 | 123.7 |
| R717 | 64301-123 | RES CHIP | 12k | +/-1% | 0.1W | Side 2 | 16.0 | 121.9 |
| R718 | 64301-154 | RES CHIP | 150k | +/-1% | 0.1W | Side 2 | 10.0 | 122.8 |
| R722 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | Side 2 | 6.1 | 152.8 |
| R723 | 64301-223 | RES CHIP | 22k | +/-1% | 0.1W | Side 2 | 8.1 | 153.6 |
| R724 | 64301-333 | RES CHIP | 33k | +/-1% | 0.1W | Side 2 | 9.4 | 153.6 |

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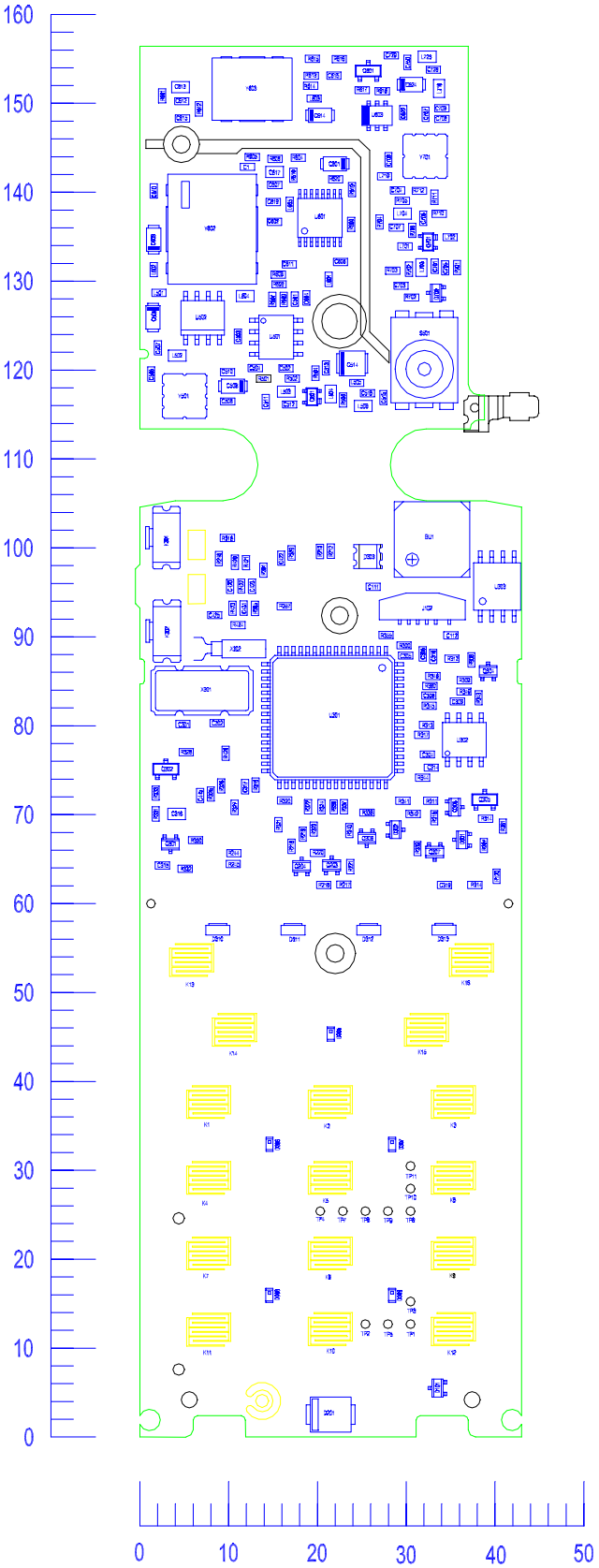
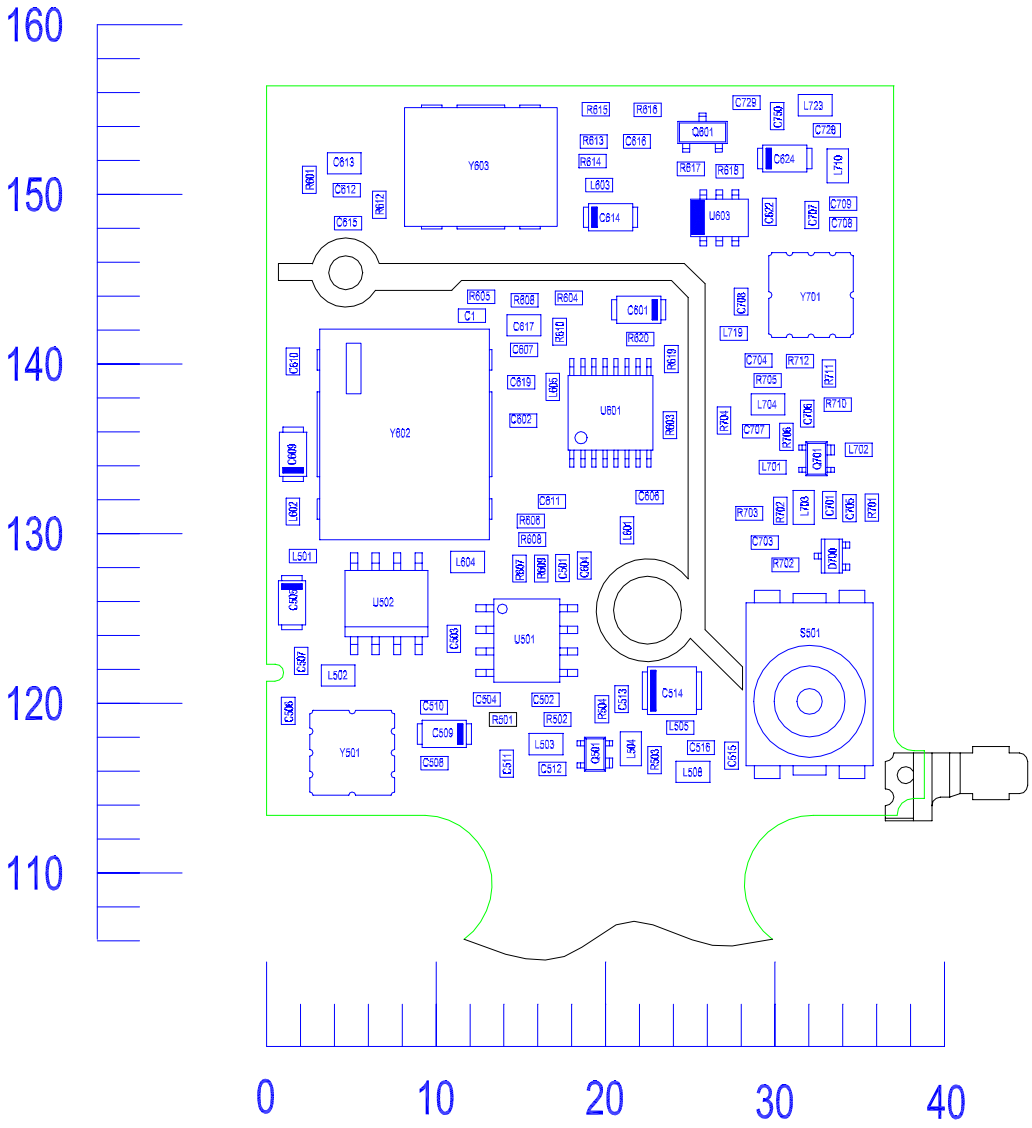
|---|---|---|---|---|---|---|---|---|---|
| R725 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | | Side 2 | 12.9 | 147.0 |
| R726 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | | Side 2 | 2.4 | 154.0 |
| R727 | 64301-393 | RES CHIP | 39k | +/-1% | 0.1W | | Side 2 | 2.0 | 132.2 |
| R728 | 64301-153 | RES CHIP | 15k | +/-1% | 0.1W | | Side 2 | 3.3 | 124.4 |
| R729 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | | Side 2 | 2.1 | 123.7 |
| R730 | 64301-102 | RES CHIP | 1k0 | +/-1% | 0.1W | | Side 2 | 4.3 | 132.2 |
| R731 | 64301-222 | RES CHIP | 2k2 | +/-1% | 0.1W | | Side 2 | 27.3 | 153.0 |
| R732 | 64301-391 | RES CHIP | 390R | +/-1% | 0.1W | | Side 2 | 32.3 | 149.2 |
| R733 | 64301-103 | RES CHIP | 10k | +/-1% | 0.1W | | Side 2 | 6.4 | 134.1 |
| R734 | 64301-470 | RES CHIP | 47R | +/-1% | 0.1W | | Side 1 | 35.0 | 135.0 |
| | | | | | | | | | |
| S0301 | 74001-001 | SWITCH | | | | | Side 1 | 3.0 | 101.1 |
| S0302 | 74001-001 | SWITCH | | | | | Side 1 | 3.0 | 90.7 |
| S0501 | 73103-001 | CONNECTOR 12 COAX | | | | | Side 1 | 32.0 | 121.1 |
| | | | | | | | | | |
| U201 | 51101-001 | IC-PWR | | | | TPS9104IPTR | Side 2 | 9.7 | 65.8 |
| U202 | 52201-001 | IC DIG 74VHC595MTC | | | | 74VHC595MTC | Side 2 | 22.3 | 72.0 |
| U203 | 50001-001 | IC-REG INV | | | | MAX868EUB | Side 2 | 33.8 | 66.8 |
| U204 | 51103-001 | IC-REG LDO 5.0V 0,25-1A | | | | TPS7250QD | Side 2 | 32.4 | 76.4 |
| U301 | 52001-001 | IC-MICROCONTR. 8-BIT | | | | ATMEGA103L-4A1 | Side 1 | 21.7 | 80.9 |
| U302 | 52101-001 | EEPROM 8k x 8 bits | | | | AT24C64N-10SI-2.7 | Side 1 | 36.5 | 78.4 |
| U303 | 52901-001 | IC-MICROCONTR Programmed | | | | 52901-001 | Side 1 | 40.2 | 95.7 |
| U401 | 51202-001 | IC AUDIO PROCESSOR | | | | AK2339 | Side 2 | 12.1 | 93.2 |
| U501 | 49201-001 | IC ATTENUATOR VARIABLE | | | | AT113 | Side 1 | 15.3 | 123.7 |
| U502 | 49301-001 | IC-AMPL 3V PWR | | | | MRFIC2006 | Side 1 | 7.1 | 125.9 |
| U503 | 51302-001 | IC-OPAMP | | | | MAX4165EUK-T | Side 2 | 11.4 | 118.4 |
| U601 | 49001-001 | IC-DUAL SYNTHESISER 1,1G/ | | | | LMX2335LTM | Side 1 | 20.3 | 137.1 |
| U602 | 51102-001 | IC-REG LDO 3.0V | | | | TK11230BMCL | Side 2 | 23.2 | 119.1 |
| U603 | 51102-001 | IC-REG LDO 3.0V | | | | TK11230BMCL | Side 1 | 26.7 | 148.6 |

| | | | | | | |
|---|---|---|---|---|---|---|
| U701 | 49101-001 | IC-FM RECEIVER LQFP-32 | MC13150FTB | Side 2 | 11.1 | 129.6 |
| X0301 | 58001-001 | CRYSTAL 4.80 MHz CS20 | | Side 1 | 7.0 | 84.0 |
| X0302 | 58901-001 | MS1V-TK 32.768KHZ 12.5PF | | Side 1 | 10.7 | 88.7 |
| Y501 | 60905-001 | FILTER-SAW TX | | Side 1 | 5.0 | 117.1 |
| Y502 | 60904-001 | FILTER-SAW RX | | Side 2 | 33.3 | 126.7 |
| Y503 | 60905-001 | FILTER-SAW TX | | Side 2 | 31.4 | 117.2 |
| Y601 | 63901-001 | OSC-VC/TCXO14.85MHZ, Sa | | Side 2 | 29.8 | 136.2 |
| Y602 | 63101-001 | VCO TX NORDIC 12,4x10MM | | Side 1 | 8.1 | 135.8 |
| Y603 | 63102-001 | OSC-RX VCO 509MHZ, NORDIC | | Side 1 | 12.7 | 151.7 |
| Y701 | 60904-001 | FILTER-SAW RX | | Side 1 | 32.1 | 144.1 |
| Y702 | 60002-001 | FILTER-IF 450KHZ | | Side 2 | 13.2 | 141.6 |
| Y703 | 60002-001 | FILTER-IF 450KHZ | | Side 2 | 20.6 | 139.9 |
| Y704 | 60001-001 | FILTER-IF 45MHZ 4-POL | | Side 2 | 18.4 | 150.8 |




**PCB Assembly**
**Side 1**




# PCB Assembly
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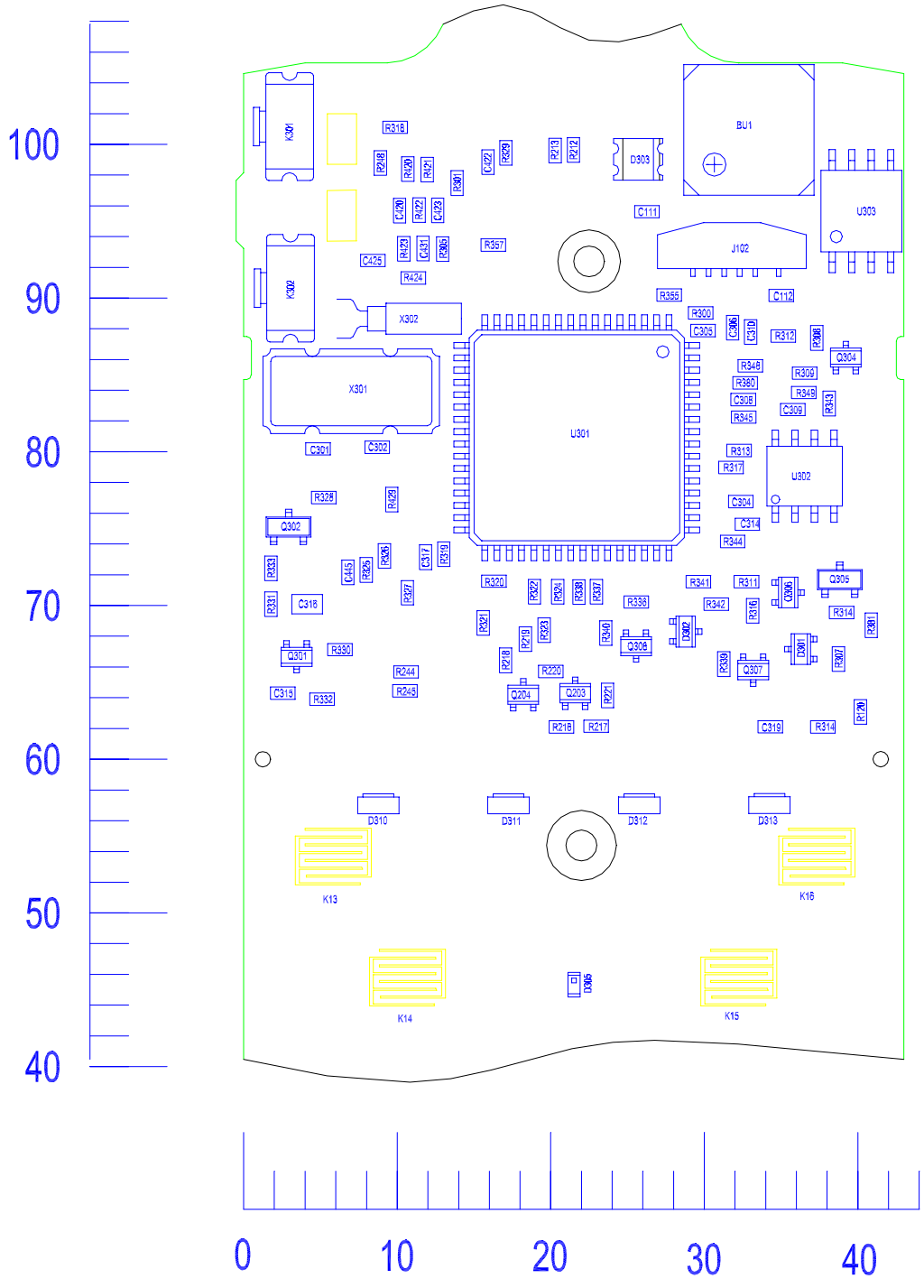


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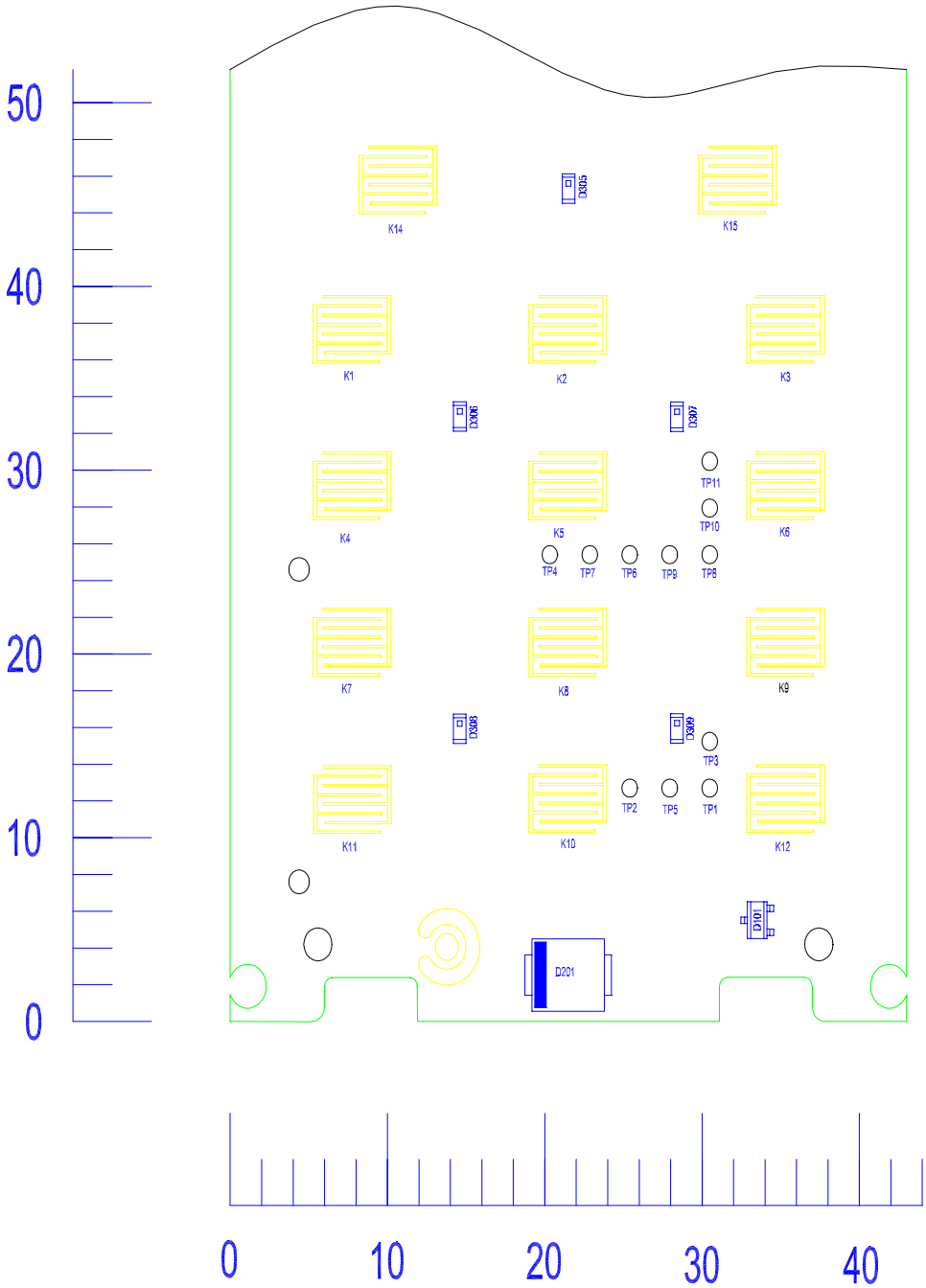


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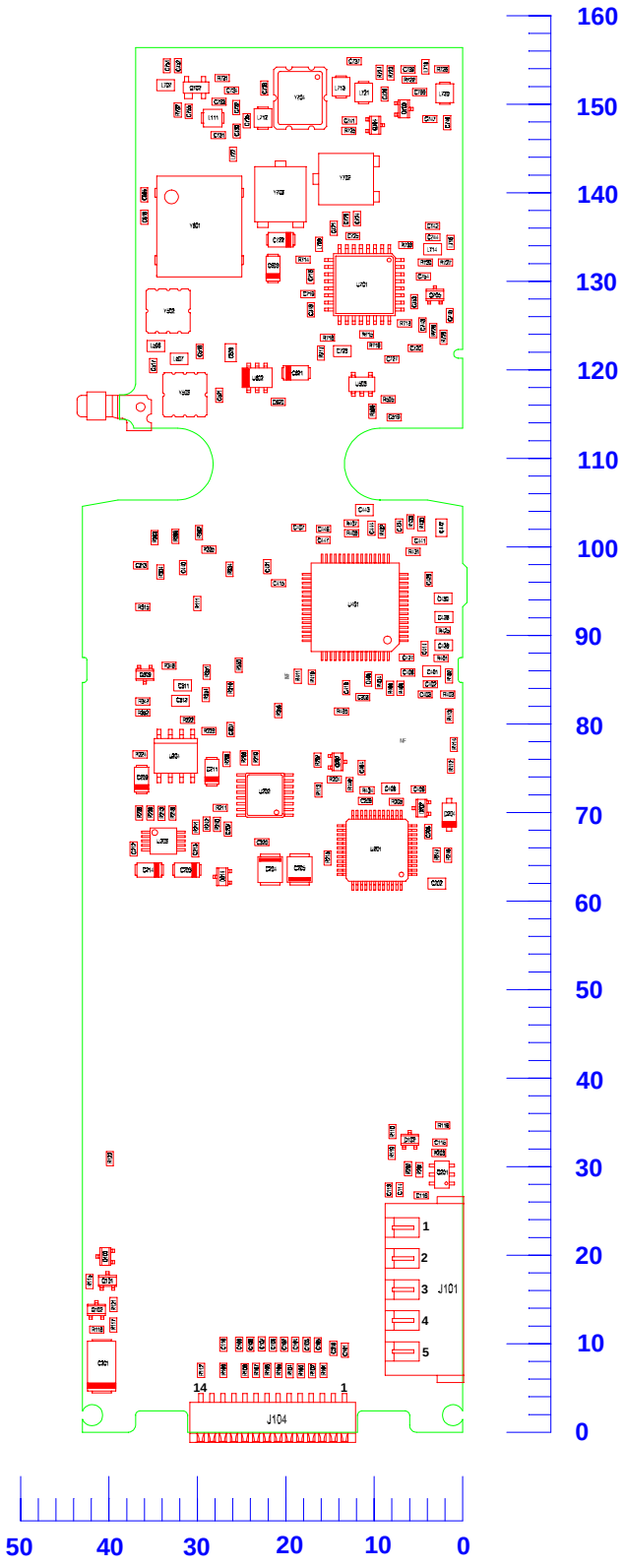
# Side 1 - Part 3

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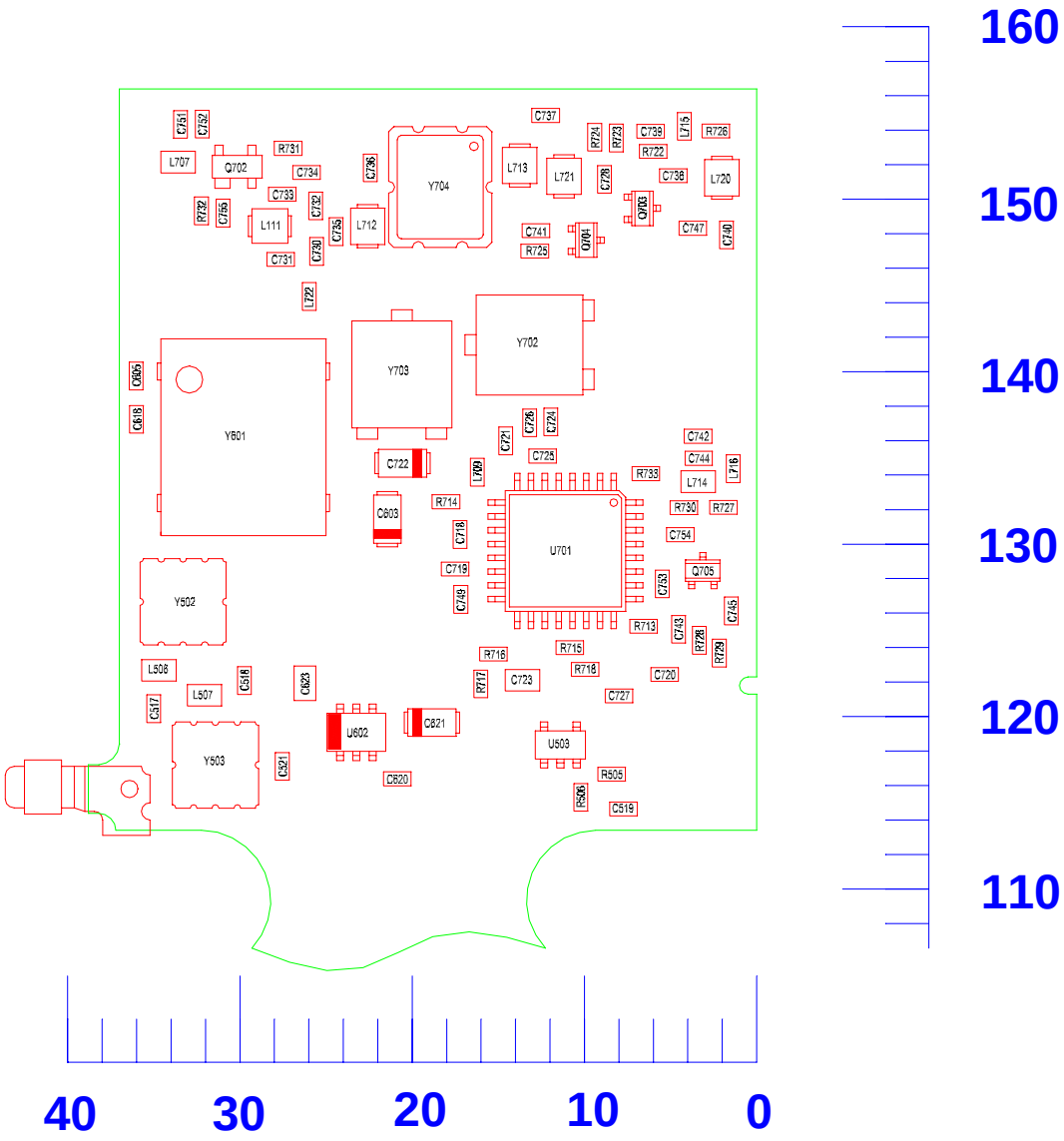
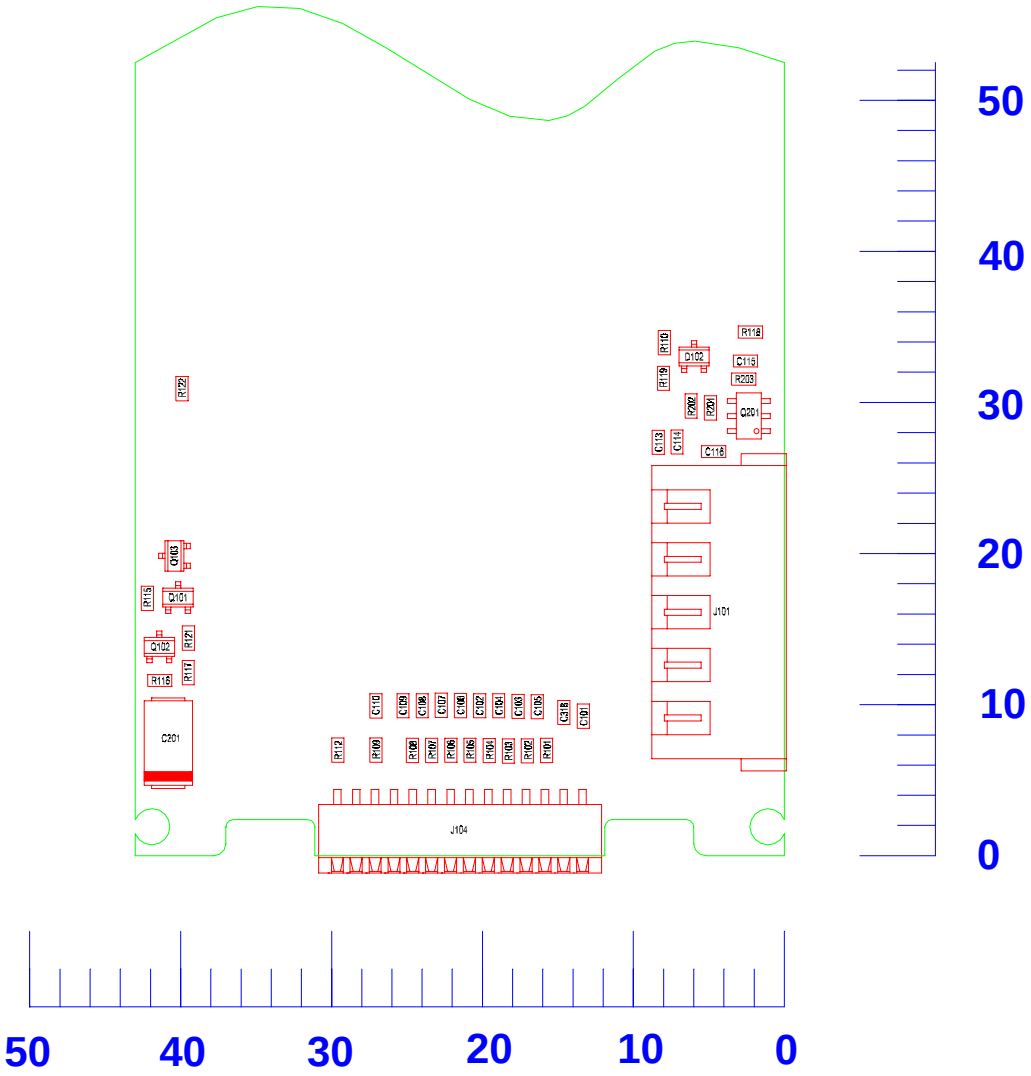



# PCB Assembly
# Side 2 - Part 1

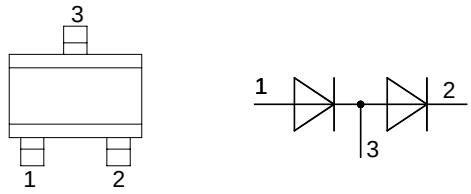

# PCB Assembly

# Side 2 - Part 2

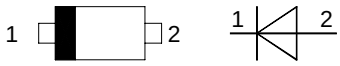



# PCB Assembly

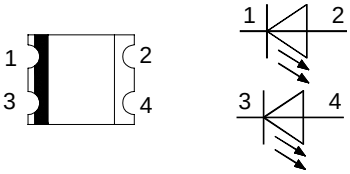
# Side 2 - Part 3



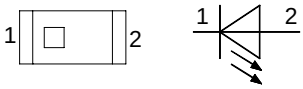

BAV99W
SOT 323



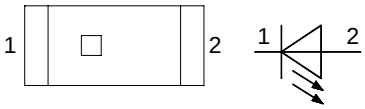

MBR0520LT1
SOD-123



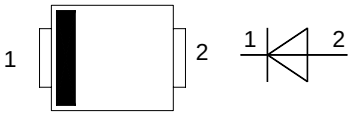

CL-155UR/G-D-T



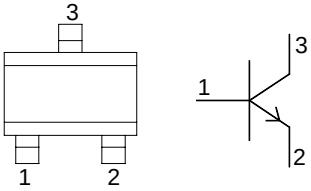

CL-190YG-CD-T



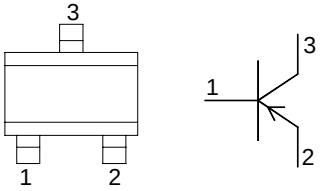

CL-220YG-C-TS




STPS340U
SMB

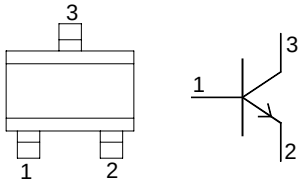



BC848CW
SOT-323

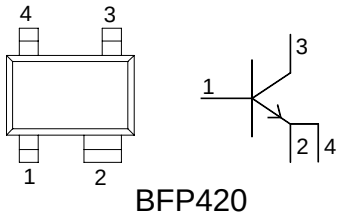



BC857BW
SOT-323

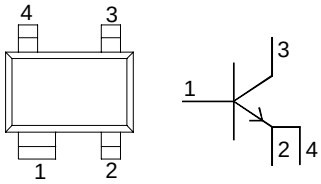
**Device Pin Outs**
**Sheet 1 of 5**



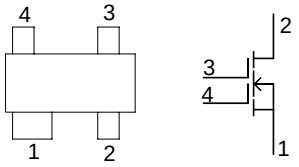

BRF92AW
SOT-323



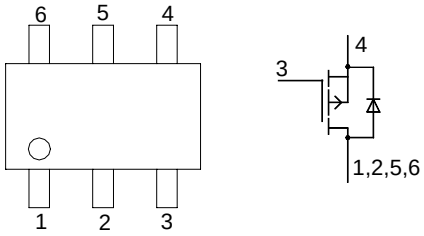

BFP420
SOT-343



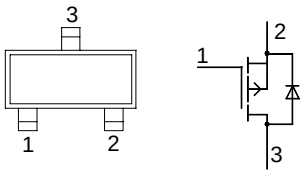

BFG10W/X
SOT-343



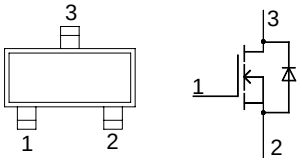

CF739
SOT-143




Si3443DV
TSOP-6

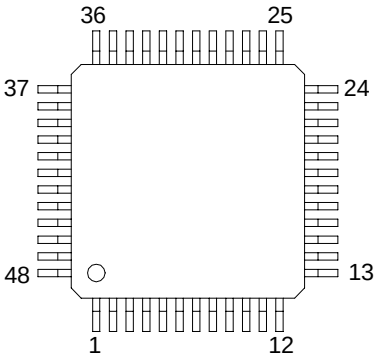



TP0101T
SOT-23

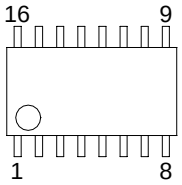



TN0200T
SOT-23

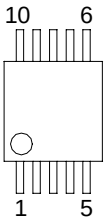
**Device Pin Outs**
**Sheet 2 of 5**



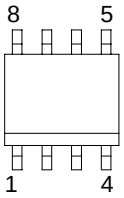

TPS9104IPT
QFP48



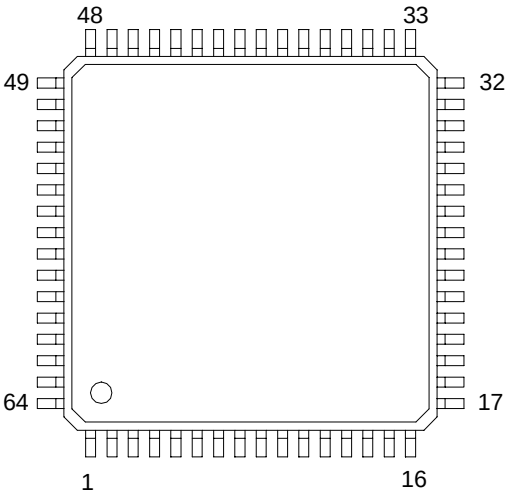

74VHC595MTC
TSSOP-16



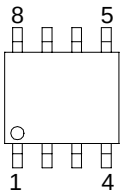

MAX868EUB
10 uMAX




TPS7250QD
R-PDS0-G8

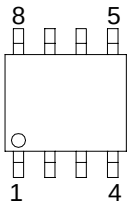



ATmega103L-4A1
TQFP-64

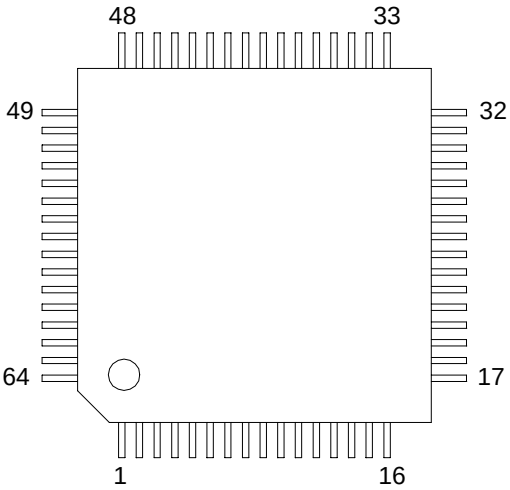



AT24C64N-10SI-2.7
SOIC-8

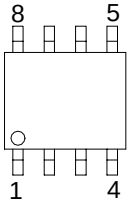
**Device Pin Outs**
**Sheet 3 of 5**



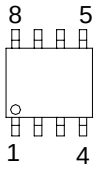

52901-001
SOIC-8



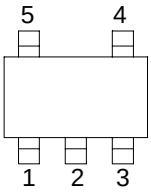

AKM2339
LQFP-64



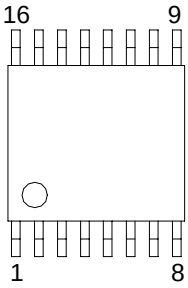

AT-113
SOIC-8




MRFIC2006
SO-8

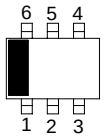



MAX4165EUK-T
SOT-23-5

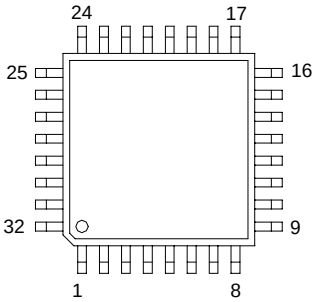



LMX2335LTM
MTC16

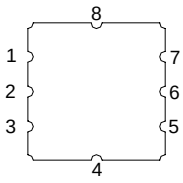
**Device Pin Outs**
**Sheet 4 of 5**



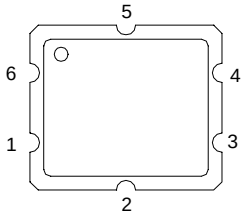

TK11230BMCL
SOT-23L



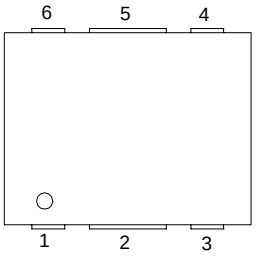

MC13150FTB
LQFP-32



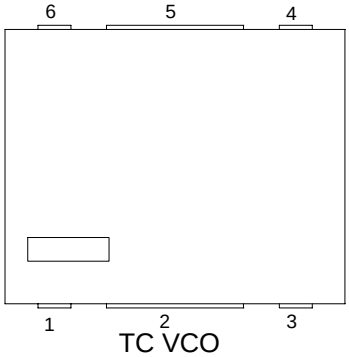

SAW Filter



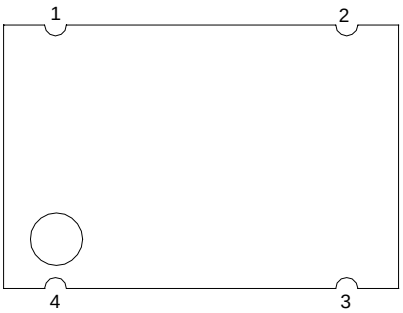

45 MHz Filter



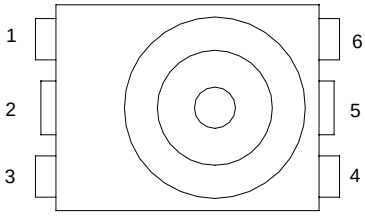

RX VCO




TC VCO




VCTCXO




Antenna Connector

**Device Pin Outs**
**Sheet 5 of 5**

# 14 Ordering Spare Parts

Not yet written

# 15 Returning Units/Assemblies to Tellit Communications Limited

Not yet written

# 16 Service Reports

Not yet written

# 17 A66 BLOCK DIAGRAM DESCRIPTION

## Introduction

**When reading this section reference should be made to the Block Diagram Figure 17-1.**

17.1 Transmitter

Specification

Direct generation of the final transmit frequency from ganged synthesiser U601.
Frequency modulation by means of the modulation input to the TX VCO.

Glossary

VCO (Y602)

Produces the TX carrier frequency. Outputs a power level of –8 dBm.

Attenuator (U501)

Provides gain control, under command of the microprocessor

Gain Controlled Amplifier (U502)

Provides power gain and gain control under command of the microprocessor.

Band Pass Filter (Y501)

Attenuates noise side bands of the TX VCO occurring within the RX frequency band
.

Power Amplifier (Q501)

Provides power gain to a level of approximately 200 mW

Duplexer (Y503 & Y502)

Comprises 2 band pass filters. Y503 passes the TX band of frequencies. Y502 passes the RX band of frequencies. Thus the transmitter and receiver may share a common antenna.

17.2 Receiver

Specification

Dual conversion superhetrodyne. Uses Surface Acoustic Wave (SAW) filters at the receive frequency, a quartz filter at the 1$^{st}$ IF frequency and ceramic filters at the 2$^{nd}$ IF frequency. 1$^{st}$ local oscillator frequency generated by means of a synthesiser under the command of the microprocessor. 2$^{nd}$ Local Oscillator generated from the 14.85 MHz VTXCO by means of a X3 frequency multiplier stage.

Glossary

LNA (Q701)

Provides low noise amplification of the receive band of frequencies

Band Pass Filter (Y701)

Attenuates received signals out side of the receive band of Frequencies.

1st Mixer (Q702)

Down converts the selected receive frequency to the 1st IF frequency of 45 MHz. Local oscillator injection frequency is 45 MHz above the selected receive channel.

1st IF Band Pass Filter (Y704)

Selects the 45 MHz component of the output of the 1st Mixer. Provides adjacent channel rejection.

1st IF Amplifier (Q703 & Q704)

Provides low noise amplification of the 1st IF.

2nd Mixer, 2nd IF Amplifier, Limiter, Demodulator & RSSI (U701

Down converts the 1st IF signal to the 2nd IF frequency of 450 kHz. Provides further adjacent channel rejection by means of Band Pass Filter Y703.

2nd IF Amplifier Provides gain at 2nd IF frequency with adjacent channel rejection by means of Band Pass filter Y704.
Provides amplitude limiter in order to remove amplitude modulation from the received signal and provide constant signal amplitude to the Demodulator stage.
Demodulator recovers the audio signal from the frequency modulated received carrier.
Receive Signal Strength Indicator (RSSI) produces a dc level proportional to the received signal carrier level.

2nd Local Oscillator Frequency Multiplier (Q705)

Multiplies the VTXCO frequency of 14.85 MHz by a factor of 3 so as to produce the required 2nd local oscillator frequency of 44.55 MHz.

17.3 Synthesiser

RX

Runs at a frequency of 45 MHz above the required receive frequency.
The VCO's output frequency is controlled by a control voltage derived from the RX Phased Locked Loop (RX PLL) via a low pass filter.
A sample of the RX VCO output is fed to the Phase Lock Loop (RX PLL).
The PLL compares the VCO frequency, divided down by a ratio determined on command from the microprocessor, with the frequency of the Voltage Tuned Crystal Oscillator (VTXCO) and produces a control voltage.
The control voltage causes the VCO to phase lock to the VTXCO frequency.

TX

Runs at the transmitter final frequency.
The VCO's output frequency is controlled by a control voltage derived from the TX PLL via a low pass filter.
A sample of the TX VCO output is fed to the TX PLL.
The TX PLL compares the VCO frequency, divided down by a ratio determined on command from the microprocessor, with the frequency of the VTXCO and produces a control voltage.
The control voltage causes the VCO to phase lock to the VTXCO frequency.
A separate modulation input to the VCO, derived from the TX Base Band circuit, produces frequency modulation of the VCO output.

Control

Interfaces to the SPI buss so as to enable control of the synthesiser by the microprocessor.

+3VIF Regulator

A 3V linear voltage regulator U603 provides a 3 V dc supply used to power the IF Demodulator (U401). This regulator is enabled under microprocessor control via line 3V_IF_EN.

+3VRX Switch

A MOSFET switch (Q602) enabled under control of the microprocessor provides +3V to power the receiver front-end.

+3VTX

A 3V linear voltage regulator U602 provides 3 V dc supplies used to power the low-level stages of the transmitter. ). This regulator is enabled under microprocessor control via line 3V_TX _EN.

17.4 BaseBand Processor

Receive Audio Path

Accepts audio from the demodulator: -
1/ Provides a –6-dB/octave de-emphasis over the audio frequency range of 300 Hz to 3.4 kHz.
2/ Provides band pass filter having a pass band of 300 Hz to 3.4 kHz.
3/ Provides an expander selectable under control of the microprocessor. The expander provides a 1:2 expansion of the RX audio (i.e. a 1-dB step in the audio level into the expander results in a 2-dB step in the output level from the expander).
4/Buffer amplifiers - one to drive the Speaker Amplifier (part of U201) – the other to drive the RX_OUT line to the I/O connector.

Transmit Audio Path

Selects TX audio source either from the Microphone Amplifier or the TX_IN line of the I/O connector under control of the microprocessor: -
1/ Provides band pass filtering having a pass band of 300 Hz to 3.4 kHz.
2/ Provides a compressor selectable under control of the microprocessor. The compressor provides a 2:1 compression of the TX audio (i.e. a 2-dB step in the audio level into the compressor results in a 1-dB step in the output level from the compressor).
3/ An emphasis circuit providing a +6 dB/octave emphasis over the frequency range of 300 Hz to 3.4 kHz.
4/ An amplitude limiter which prevents over modulation of the transmitter carrier.
5/ The output of the limiter drives the modulation input of the TXVCO.

FFSK RX

Provides demodulation of the 1200-baud Fast Frequency Shift Keyed (FFSK) data transmissions used to provide data signalling between the base station and the mobile station.

FFSK TX

Provides modulation of the 1200 baud FFSK data transmission used to provide data signalling between the mobile station and the base station.

Ø Signal

The Ø Signal, comprising a tone at a frequency of one of 4 possible frequencies (3055, 3985, 4015 and 4045 Hz), is originated at the base station transmitter under the control of the Mobile Telephone Exchange (MTX). The use of 4 alternative Ø -signals allows the

mobile to differentiate between channels in use at the local cell and channels used at more distant cells. When received at the mobile station it is filtered and then inserted back into the mobile station's transmission. Thus the Ø Signal is looped back to the base station receiver were it is used to assess the performance of the radio path. If the fixed part of the radio telephone system determines that the radio path performance is too poor to provide an acceptable speech quality the system will scan adjacent cell sites seeking an alternative site, thus providing improved speech quality. When an adjacent site has been located, the system initiates hand-off of the mobile to the adjacent cell on an alternative traffic channel.

8-Bit DAC

Provides digital to analogue conversion of data sent over the serial bus from the microprocessor. 3 DAC channels are provided VTXCO, POWER_CTRL and PA_Bias.

Control

Provides interface to the SPI, enabling control of the Audio Processor by the microprocessor.

## 17.5 Processor

Introduction

The processor used is the Atmel Atmega103L. This device provides the following facilities used within the phone;

- Atmel AVR® Enhanced RISC architecture.
- 121 powerful instructions – most single clock cycle execution.
- 128k bytes of in-system re-programmable flash program memory.
- SPI interface for in-system programming.
- 4k bytes of internal EEPROM.
- 4k bytes of internal SRAM.
- 32 X 8 general-purpose working registers + peripheral control registers.
- 32 X 8 programmable I/O lines, 8-output lines 8 input lines.
- Programmable serial UART + SPI serial interface.
- Fully static operation.
- RTC with separate oscillator.
- Two 8-bit Timer/Counters with separate prescaler and PWM.
- One 16-bit Timer/Counter with separate prescaler, compare, capture modes and dual 8, 9 or 10 bit PWM.
- Programmable watchdog timer with on-chip oscillator.
- On-chip analog comparator.
- 8-channel 10-bit ADC.
- Low power idle, power save and power down modes.
- Software selectable clock frequency.
- Program lock for software security.

Clock Frequencies

Two clock frequencies, selectable under software control are provided. Under normal operation the processor operates at an instruction execution cycle rate defined by the 4.8 MHz quartz crystal (X301). Whilst in sleep mode. (I.e. phone powered down,) the processor runs at a lower instruction cycle rate defined by the 32.788 kHz ceramic resonator.

External EEPROM

External EEPROM (64k) is provided by U302. This memory is used to store various user configurable settings e.g. the phone book.

SIM

The Subscriber Identification Module (SIM), comprising an 8-bit microprocessor (U303), is provided in order to prevent the illicit use of the mobile telephone's identification number. At certain stages during a mobile originated call an authentication procedure takes place. During this procedure a Secret Authentication Key (SAK), stored in the SIM is used to authenticate the use of the telephone and prevent fraud. The SAK is programmed into the SIM by Tellit during its manufacture. **In the event of the failure of the SIM a replacement SIM, programmed by Tellit, together with a replacement Rear Equipment Label, must be obtained and fitted. Associated with each programmed SIM is a serial number – the SIS number. When the SIM is replaced it will be necessary to register the SIS number of the replacement SIM with the System Operator.**

Keyboard

The Keyboard comprises an array of printed switches arranged in matrix on the PCB activated by conductive rubber pads on the keymat. The state of the switches is scanned by the microprocessor by means of column and row lines.

LCD Module

A LCD display panel-having graphics display capability is provided. The display interfaces to the microprocessor via serial clock (SCL) and serial data (SDL) lines. A series of LEDs are fitted to provide illumination for improved visibility. These also serve to illuminate the keypad.

-4.8V Generator

A voltage converter stage (U203) generates a –4.8 V supply required as a power supply to the LCD display.

17.6 Power

Speaker Amplifier

An audio frequency power amplifier located within U201 drives the speaker.

Ringer Amplifier

An audio frequency power amplifier located within U201 drives the ringer.

Reset Generator

Reset Generator circuit located within U201 provides a reset signal to the microprocessor. This causes the microprocessor to perform a power on reset initializing all I/O registers and the program counter. Once a normal power on reset has been completed, program execution proceeds with the processor in sleep mode.

+3VA Regulator

A 3V linear voltage regulator located within U201 provides the +3VA supply line.

+3VDIG Regulator

A 3V linear voltage regulator located within U201 provides the +3VDIG supply line.

8-Bit Shift Register

The 8-bit shift register (U202) decodes commands sent by the microprocessor over the serial bus. These commands are used to control the following functions:

- HI_CUR_EN
- BATT_TYPE
- 3V_IF_EN
- /3V_RX_EN
- 3V_TX_EN
- BUZZER_EN
- SPEAKER_EN

## 17.7 Connections

System Connector (J104)

A 14 pole System Connector is provided for the use of various phone accessories and to enable the configuration, programming and test and diagnostic equipment.

HOOK_C/RESET Interface

The HOOK_C/RESET interface is made up of Q101, Q103 & Q103. Signals input via the HOOK_C/Reset level are decoded into two signals zero V for actuation and –4V for programming and processor reset.

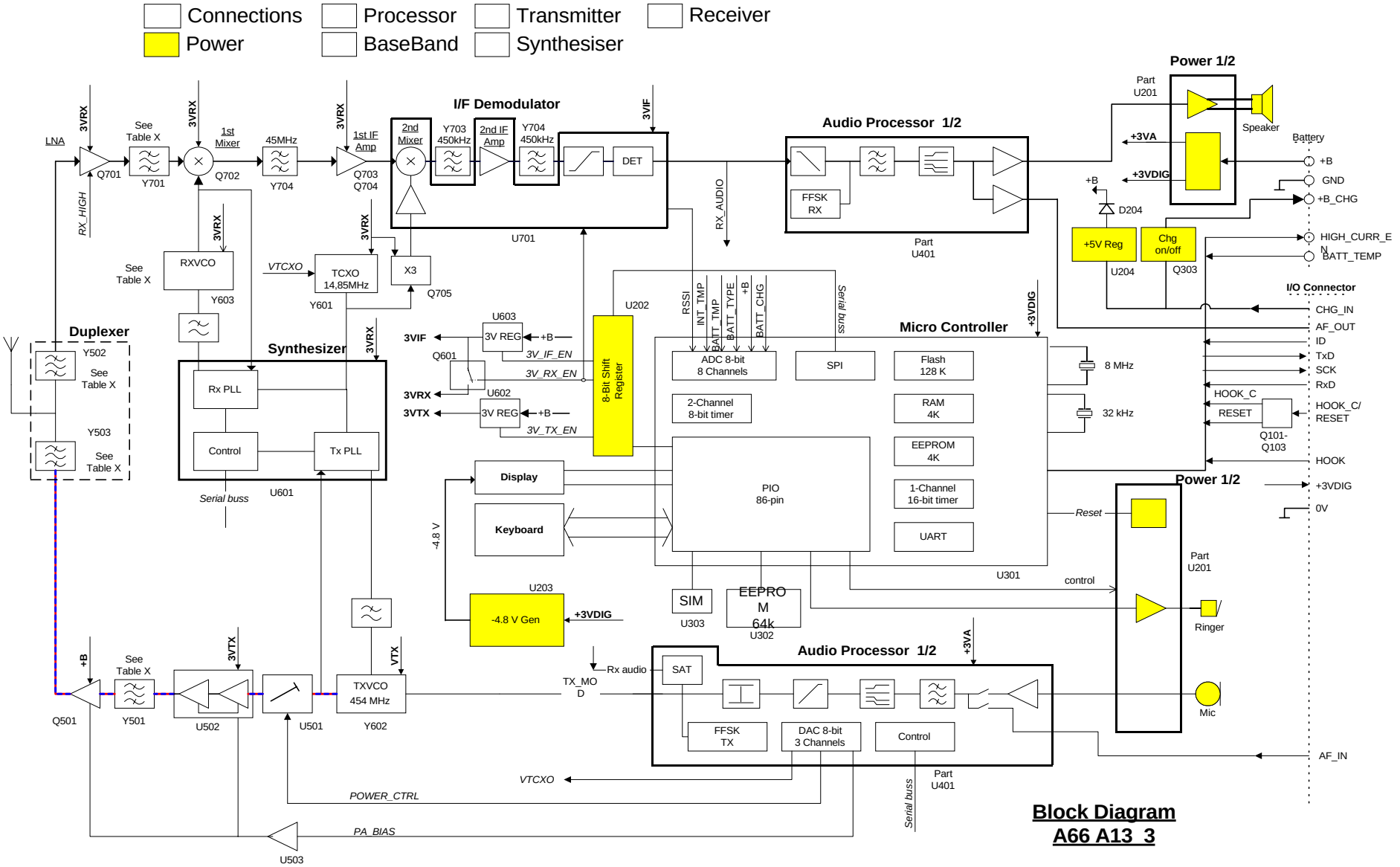

Connections
Power
Processor
BaseBand
Transmitter
Synthesiser
Receiver
I/F Demodulator
Audio Processor 1/2
Power 1/2
Micro Controller
Synthesizer
Duplexer
Audio Processor 1/2
Power 1/2
I/O Connector
Block Diagram
A66 A13_3

Figure 17-1